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Development of a 1 GS/s high-resolution sampling ADC system

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ABSTRACT

Today, many experiments in high energy physics have to handle data rates of several MHz per readout channel to reach statistical significance for the measured quantities. In addition, these experiments frequently have to deal with short analog pulses of a few nanoseconds length which may cover large dynamic ranges and which require amplitude as well as time measurements with highest accuracy. For applications of this kind fast transient recorders with very high resolution and deep on-board memory are the first choice. We have built a 16-channel 12- or 14-bit single unit VME64x/VXS sampling ADC module which may sample at rates up to 1 GS/s. Fast algorithms have been developed and successfully tested on scintillating counter detectors to implement pulse shape discrimination, constant fraction timing and gated integration.

1. Introduction

The COmmon Muon and Proton Apparatus for Structure and Spectroscopy (COMPASS) at the CERN SPS [1] is a state-of-the-art two stage magnetic spectrometer [2] with a flexible setup to allow for a rich variety of physics programs to be performed with secondary muon or hadron beams. Common to all measurements is the requirement for highest beam intensity and interaction rates with the needs of a high readout speed. Recently interest has been expressed for pursuing a dedicated measurement of generalized parton distributions (GPD) [3]. For these measurements the collaboration shall use the existing COMPASS spectrometer together with a new liquid hydrogen target, 2.4 m long, and a new recoil detector based on scintillating counters surrounding the target. The background induced by the passage of the beam through the target will yield rates of the order of a few MHz in the recoil detector counters. This imposes great demands on the digitization units and on a hardware trigger based on the recoil particle. For this purpose we have developed within the GANDALF framework a modular high speed and high resolution transient recorder system.

2. The GANDALF framework

GANDALF (Fig. 1) is a 6U VME64x/VXS carrier board which can host two mezzanine cards. It has been designed to cope with a variety of readout tasks in high energy and nuclear physics experiments. Two exchangeable mezzanine cards allow an employment of the system in very different applications such as analog-to-digital or time-to-digital conversions, coincidence matrix formation, fast pattern recognition or fast trigger generation. A schematic overview of the carrier board as transient recorder is provided in Fig. 2. The heart of the board is a VIRTEX5-SXT FPGA which is connected to the mezzanine cards by several single ended and more than 110 differential signal interconnections. The data processing FPGA can either perform complex calculations on data which have been sampled on the mezzanine cards or act as a digitizer by itself. Fast and deep memory extensions of 144-Mbit QDRII+ and 4-Gbit DDR2 RAM are connected to a second Virtex5 FPGA. Both FPGAs are linked to each other by eight bidirectional high-speed Aurora lanes.

Connected to the VXS backplane GANDALF has 16 high-speed lanes for data transfer to a central VXS switch module, where the lanes of up to 18 GANDALF modules merge. This interface can be used for continuous transmission of the analog sums and the time stamps from sampled signals to the VXS switch to form a trigger based on the energy loss and the time of flight in the recoil detector.

A dead-time free data output can either be realized by dedicated backplane link cards connected to each GANDALF P2-connector, i.e. following the 160 MByte/s SLink [4] or Ethernet protocol, or by the VME64x bus in block read mode [5] or by USB2.0 from the front panel.

3. Analog-to-digital converter

A particular type of analog mezzanine cards (AMC) is equipped with eight 12-bit (ADS5463, max. 500 MS/s) or 14-bit (ADS5474, max. 400 MS/s) sampling ADC units. The ADCs are operated at a sampling frequency of up to 500 MS/s. Two adjacent 500-MHz bandwidth analog input circuits can be interleaved to achieve an

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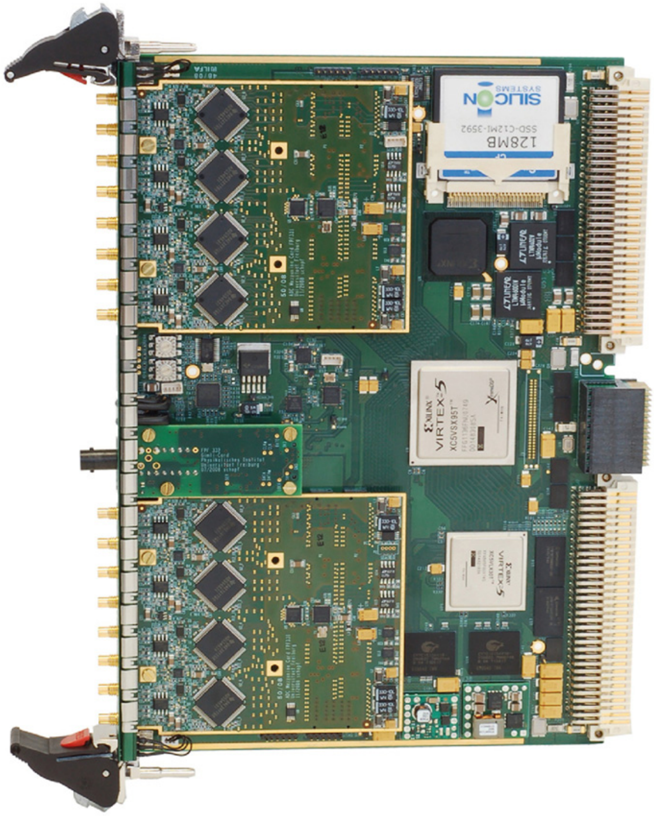

Fig. 1. Picture of the GANDALF carrier board equipped with two analog mezzanine cards. The center mezzanine card hosts an optical receiver for the COMPASS trigger and clock distribution system.

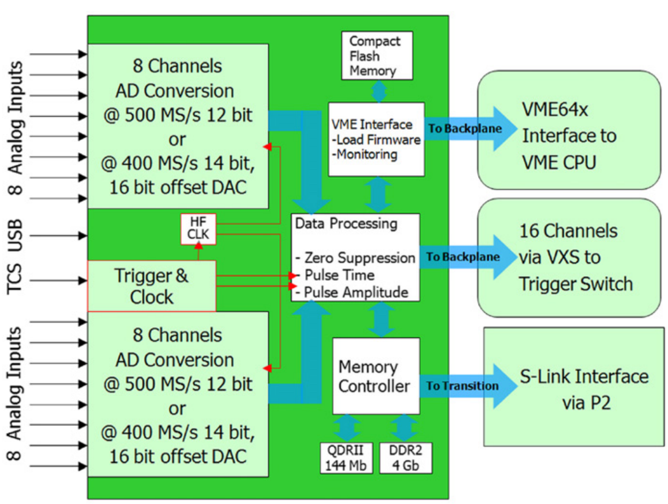

Fig. 2. Block diagram of GANDALF as a transient recorder.

effective sampling rate of 1 GS/s (800 MS/s with the ADS5474) at the cost of the number of channels per mezzanine card. The baseline of each DC-coupled single-ended signal input can be adjusted individually by 16-bit digital-to-analog converters.

On each GANDALF the high frequency sampling clocks are generated by digital clock synthesizers from a 155-MHz time multiplexed signal distributed by the COMPASS trigger and clock distribution system. Particular care has been paid to the design of the clock filter networks and the board layout to reach a time interval error smaller than 730 fs [6].

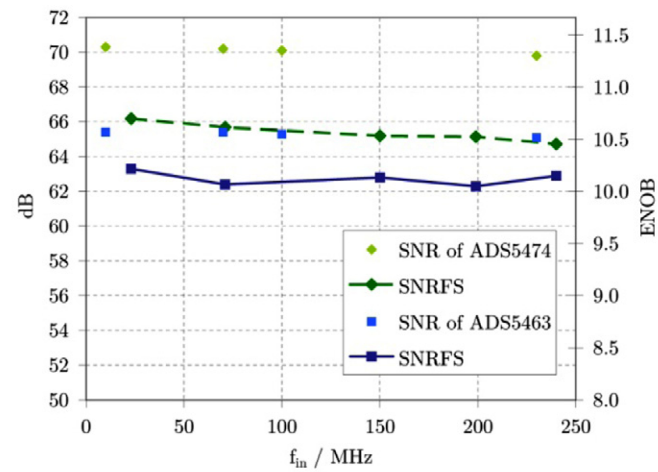

Fig. 3. Measured analog resolution of a GANDALF AMC together with its theoretical values from the ADC data sheets.

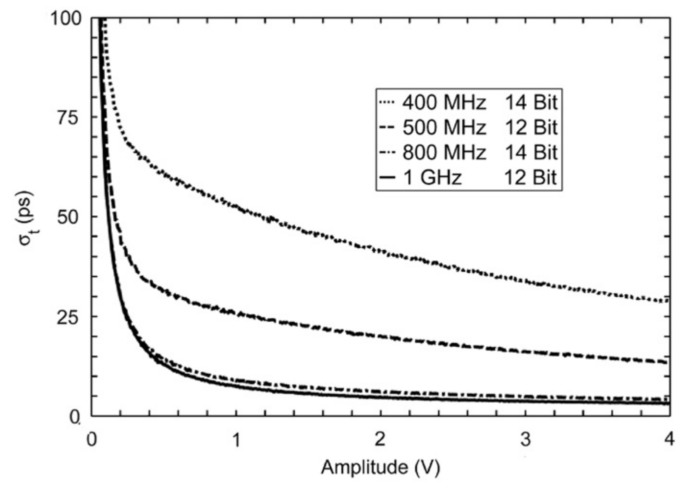

Fig. 4. With our 12-bit, 1GS/s sampling ADC a resolution of 7 ps can be achieved for pulses exceeding 25% of the dynamic range of the input signals.

4. Tests and simulation

In experimental tests performed with a high precision function waveform generator (AFG-3252) and a selection of narrow band pass filters connected directly to the AMC input we achieved a resolution on sample measurements of 10.1 ENOB (ADS5463) and 10.6 ENOB (ADS5474) full scale. These measurements are shown in Fig. 3 as a function of the frequency of the input analog signal.

From a sampled pulse the FPGA can calculate the time of its occurrence using DSP-optimized numerical algorithms. With our knowledge of the sampling resolution extensive simulations aimed at the time resolution were performed. Different algorithms were tested and optimized [7]. The resolution on the time extracted from a pulse with different amplitudes of 3 ns rise time, as expected from our detector, is shown in Fig. 4.

5. Conclusion

A low cost VME64x/VXS system aimed at digitizing and processing detector signals has been designed and implemented to our full satisfaction. The design is modular, consisting of a carrier board on which two mezzanine boards, with either analog or digital inputs can be plugged. In a forthcoming paper we will describe the realization of GANDALF as a 128-channel

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time-to-digital converter module with 100 ps digitization units, comparable to the F1-TDC chip [8], which hosts 128 channels of 500-MHz scalers at the same time.

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