



# The GANDALF High-Resolution Transient Recorder System

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University of Freiburg

DPG Münster 2011



bmb+f - Förderschwerpunkt

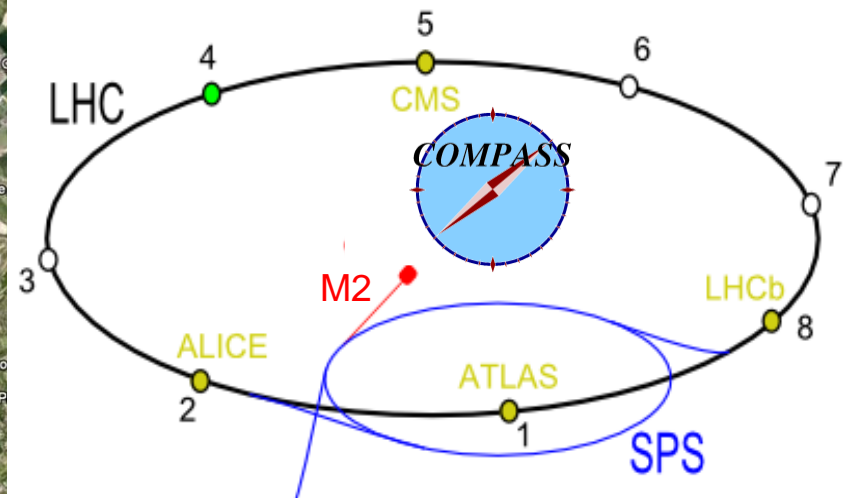
**COMPASS**

Großgeräte der physikalischen  
Grundlagenforschung



# COMPASS – Fixed Target Experiment

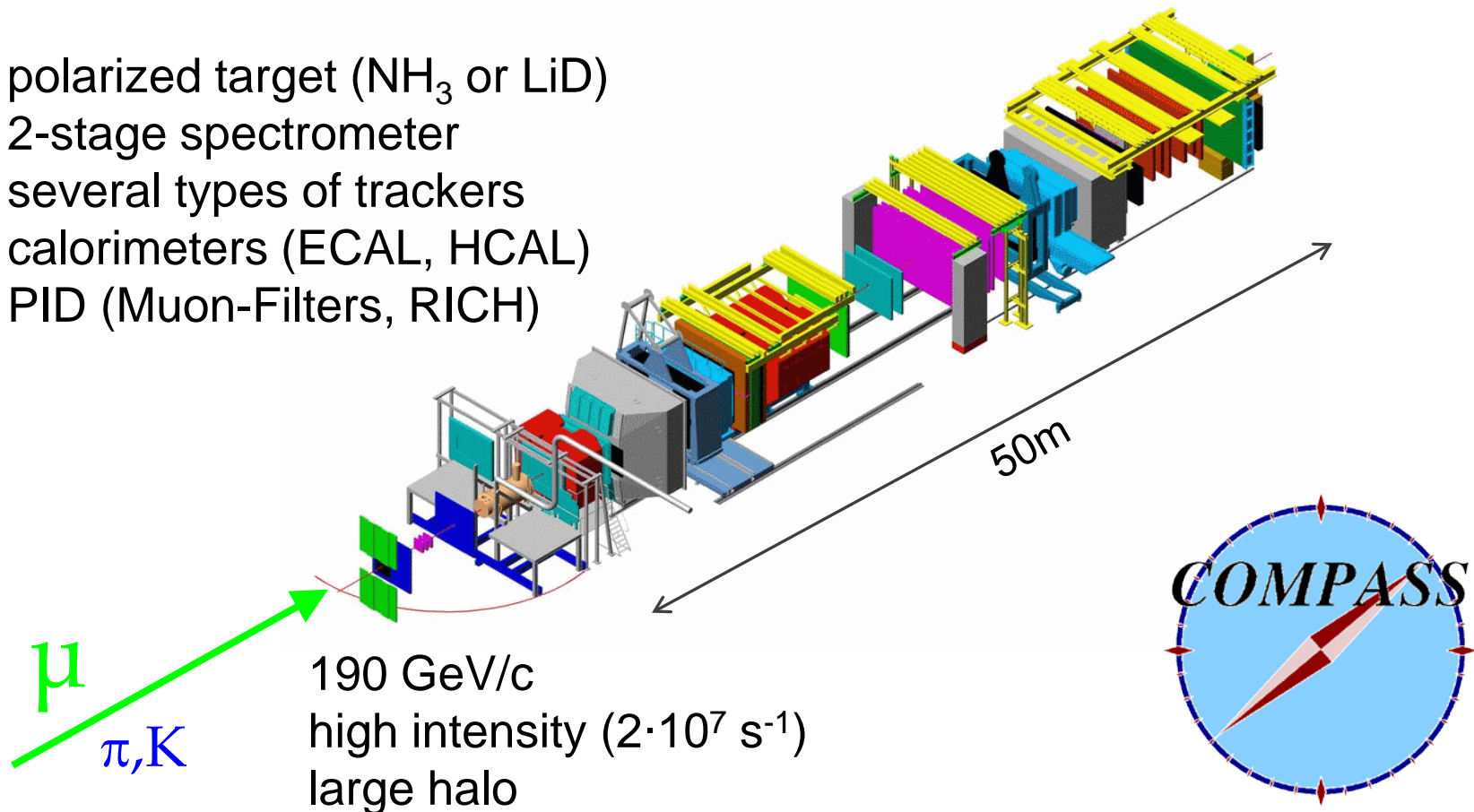
COMPASS – Experiment:  
240 physicists from  
11 countries and  
28 institutions



# COMPASS Facility (since 2002)

## Hadron Spectroscopy, Deep Inelastic Scattering

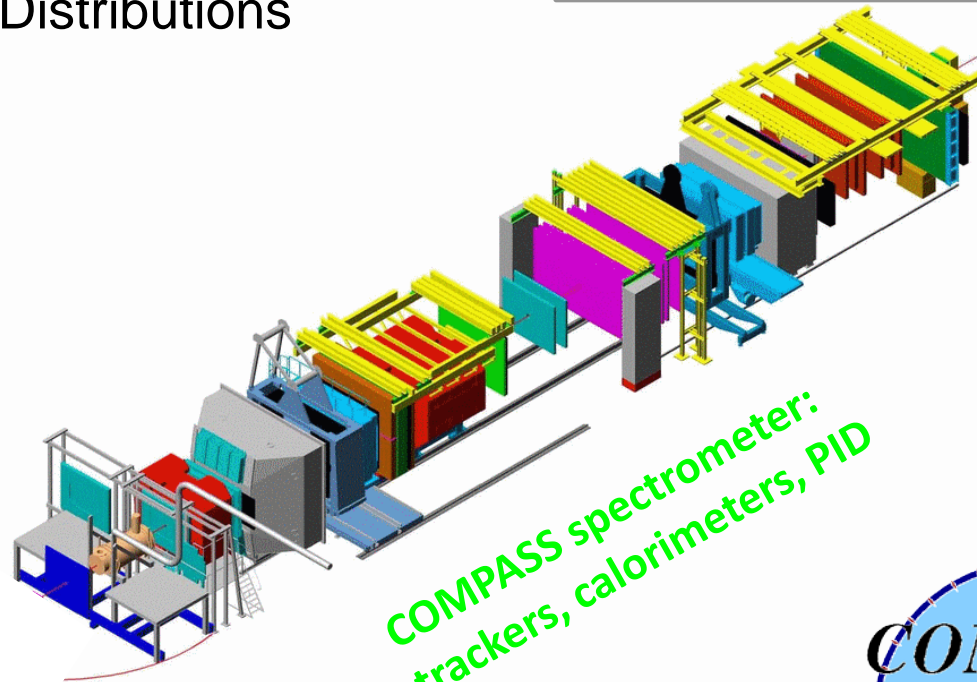
- polarized target ( $\text{NH}_3$  or  $\text{LiD}$ )
- 2-stage spectrometer
- several types of trackers
- calorimeters (ECAL, HCAL)
- PID (Muon-Filters, RICH)



# COMPASS-II Upgrade

COMPASS-II proposal: determination of  
Generalized Parton Distributions

DVCS:  $\mu p \rightarrow \mu p \gamma$



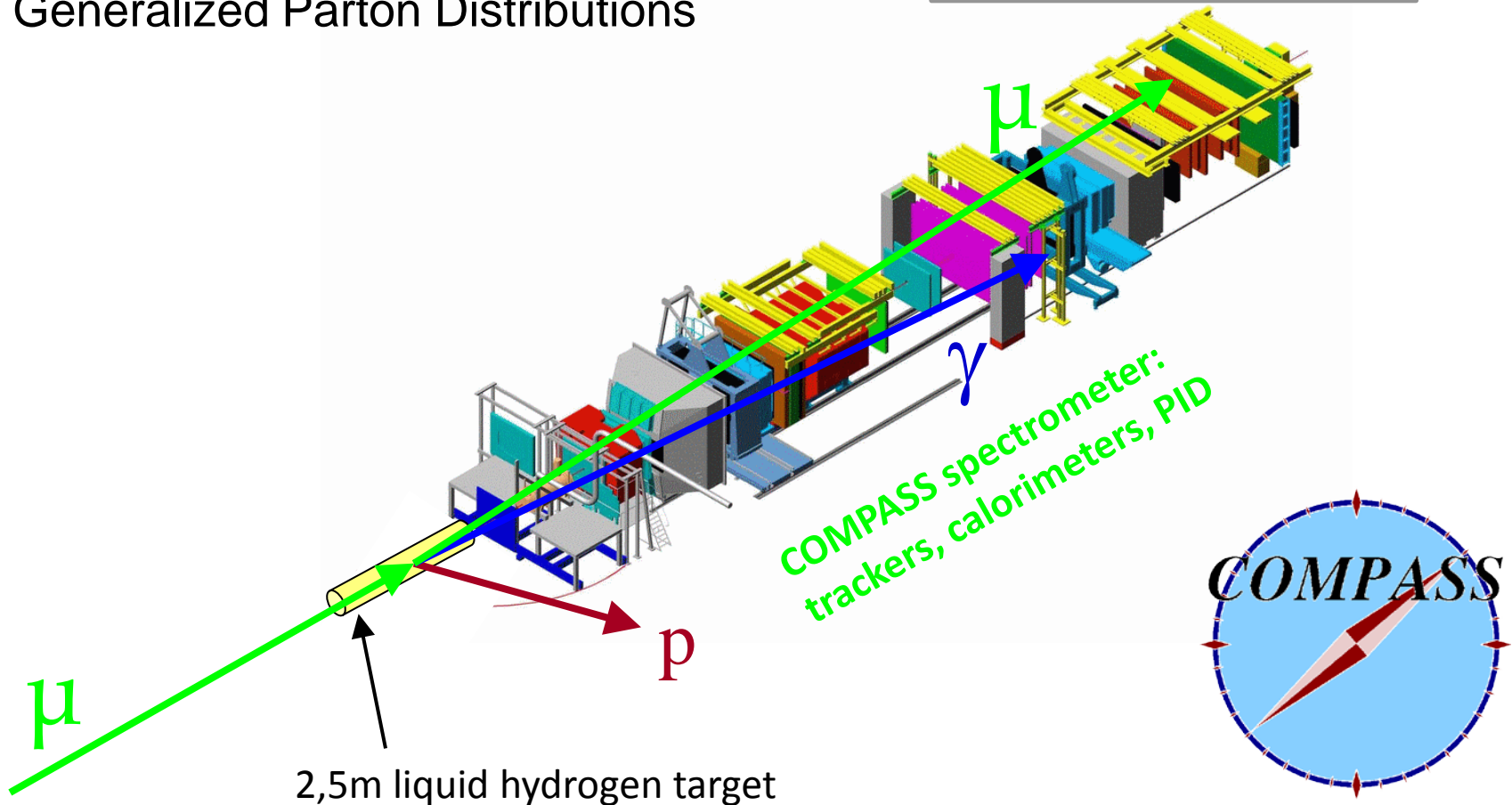
COMPASS spectrometer:  
trackers, calorimeters, PID



# COMPASS-II Upgrade

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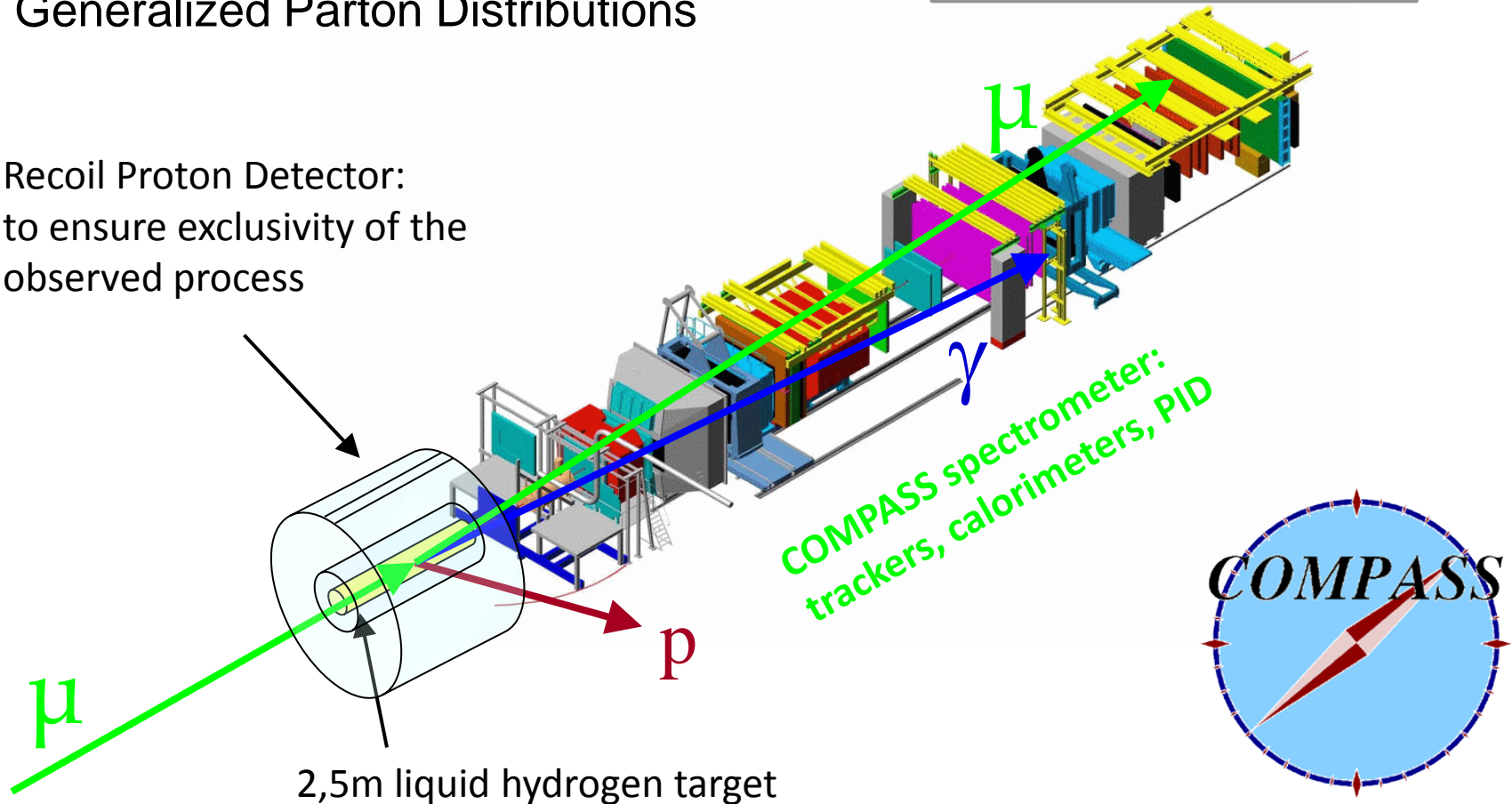


# COMPASS-II Upgrade

COMPASS-II proposal: determination of Generalized Parton Distributions

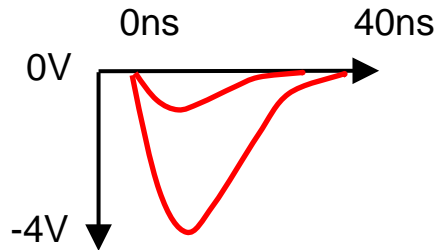
DVCS:  $\mu p \rightarrow \mu p \gamma$

Recoil Proton Detector:  
to ensure exclusivity of the  
observed process

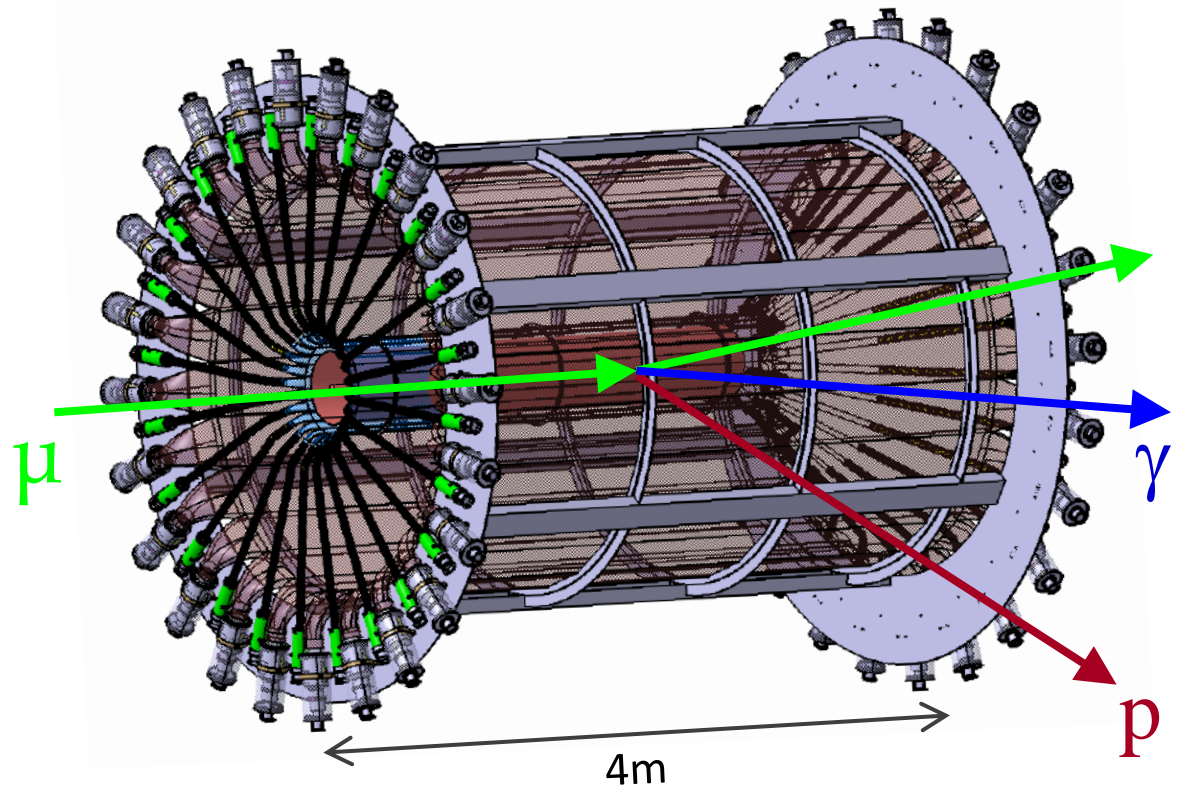
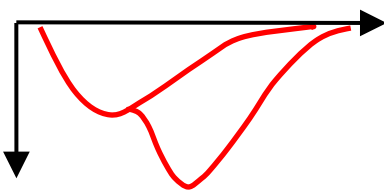


# Recoil Proton Detector (RPD)

measurement of:  
-time-of-flight ( $\sigma < 200\text{ps}$ )  
-energy deposit



high luminosity:  
separation of pile-up  
pulses is required



inner barrel (A):  $\varnothing$  0.50 m  
outer barrel (B):  $\varnothing$  2.20 m

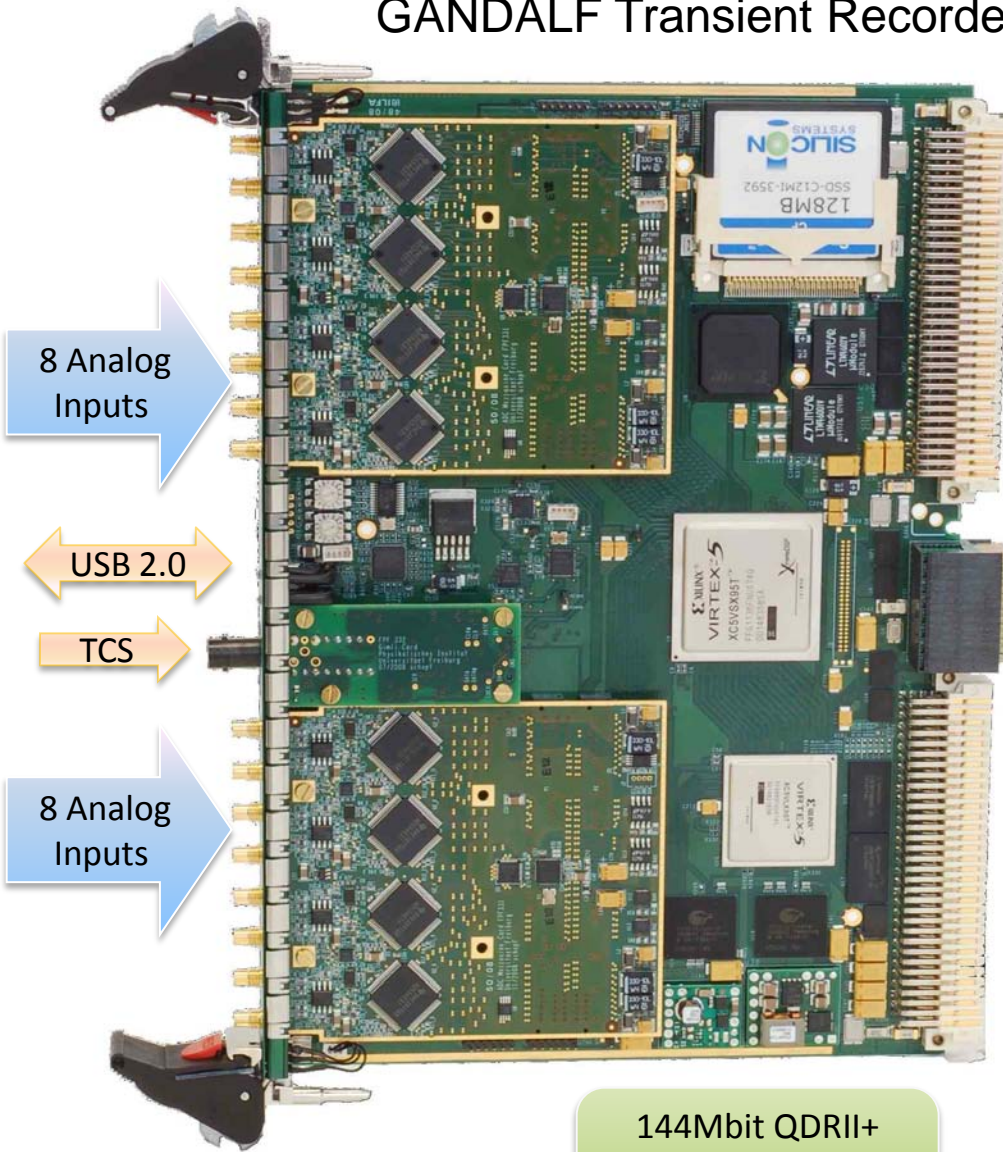
# GANDALF Transient Recorder

500MHz  
Bandwidth  
Analog Inputs

12 bit  
500MS/s ADCs

16bit DACs for  
Offset Correction

V5 SXT FPGA for  
Data Processing



8 Analog  
Inputs

USB 2.0

TCS

8 Analog  
Inputs

144Mbit QDRII+  
4Gbit DDR2  
Memories

VME64x  
Interface

VITA 41.0  
VXS Interface

S-Link Interface  
to DAQ

V5 LXT FPGA for  
Memory Control  
& Data Output



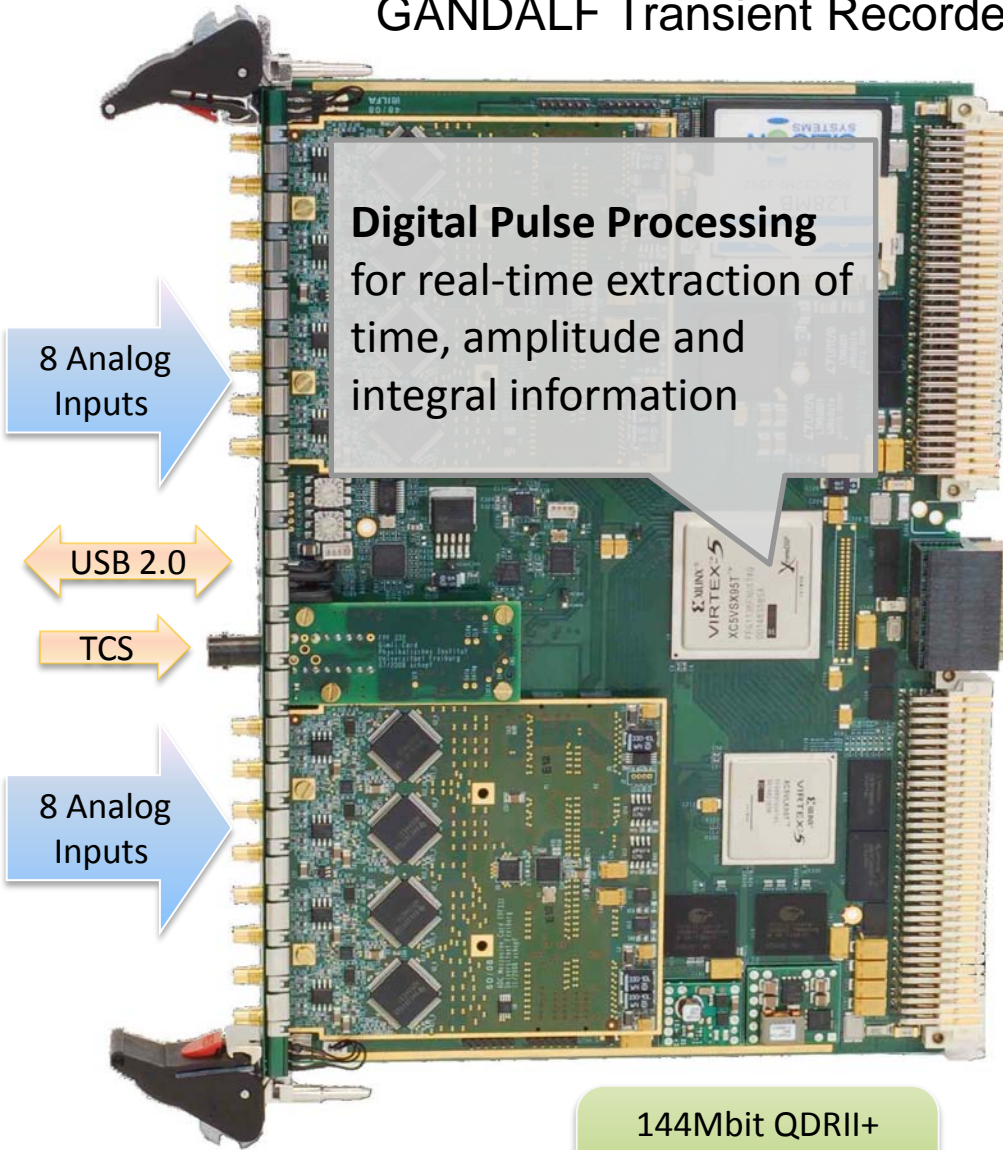
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8 Analog  
Inputs

USB 2.0

TCS

8 Analog  
Inputs

**Digital Pulse Processing**  
for real-time extraction of  
time, amplitude and  
integral information

VME64x  
Interface

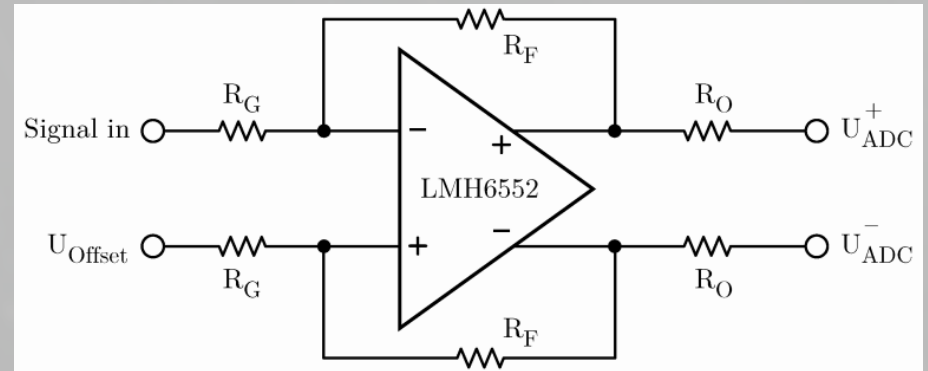
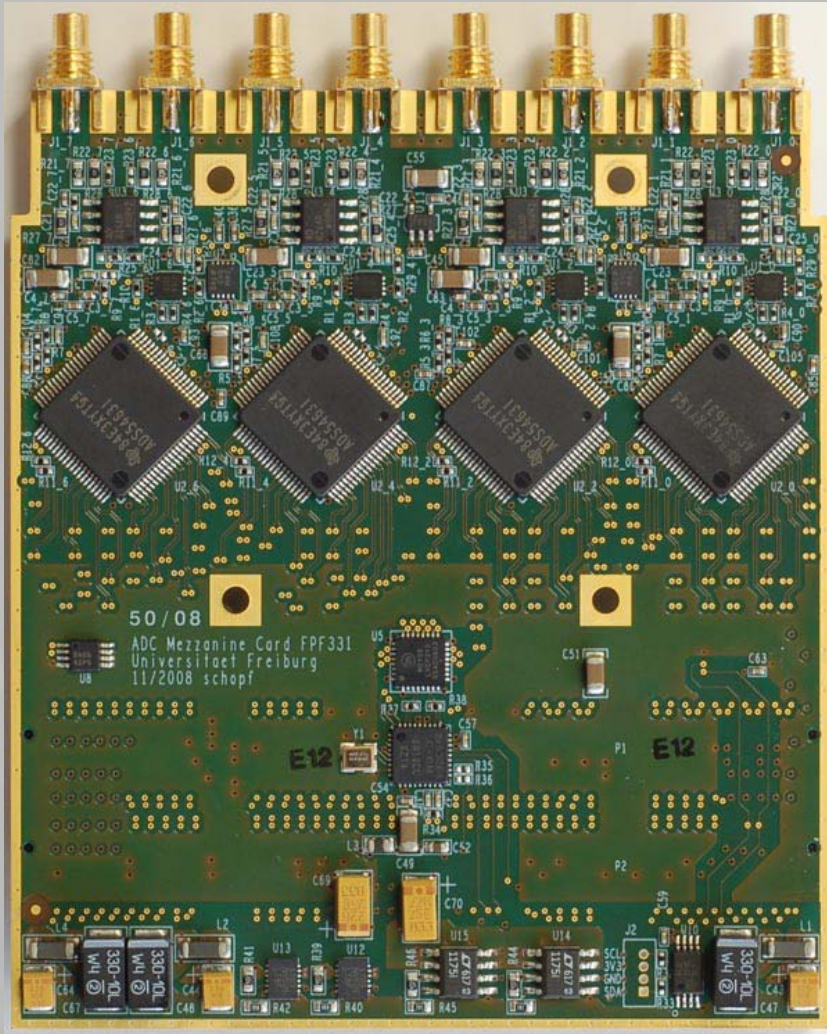
VITA 41.0  
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144Mbit QDRII+  
4Gbit DDR2  
Memories

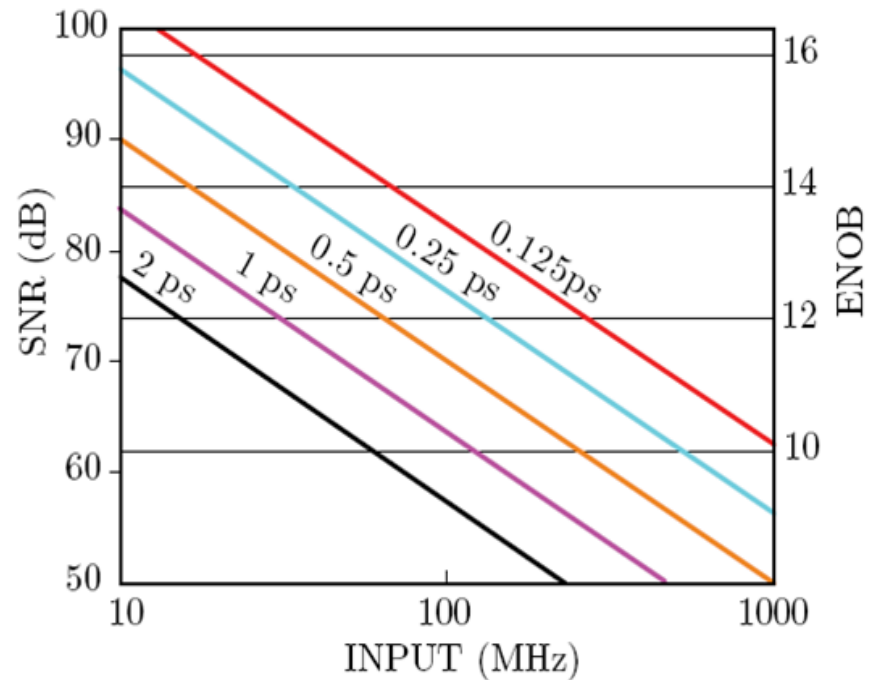
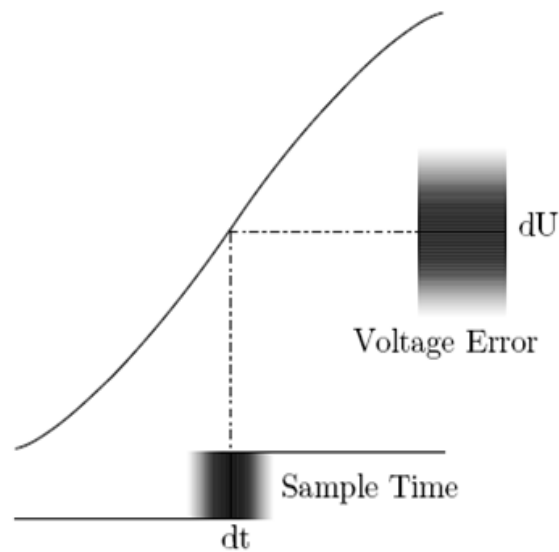
V5 LXT FPGA for  
Memory Control  
& Data Output

# ADC Mezzanine Card



- 8 ADC channels  
(12bit@500MS/s or 14bit@400MS/s)
- optional time-interleaved mode
- offsets are adjustable by DACs
- gain is adjustable by changing some resistors
- flexible input range  
(e.g. -4V..0V , -2V..+2V, -1V..0V, ...)

# Sampling Clock Requirements

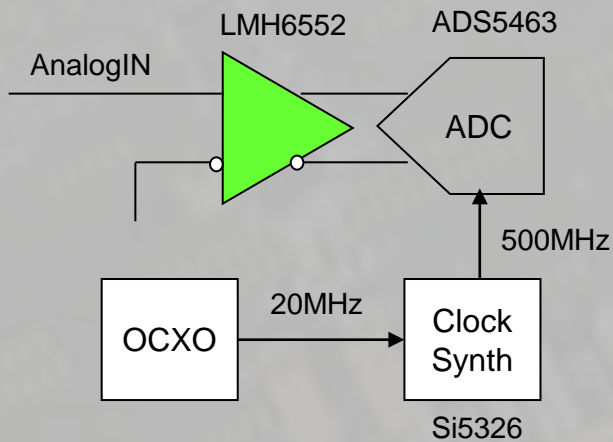
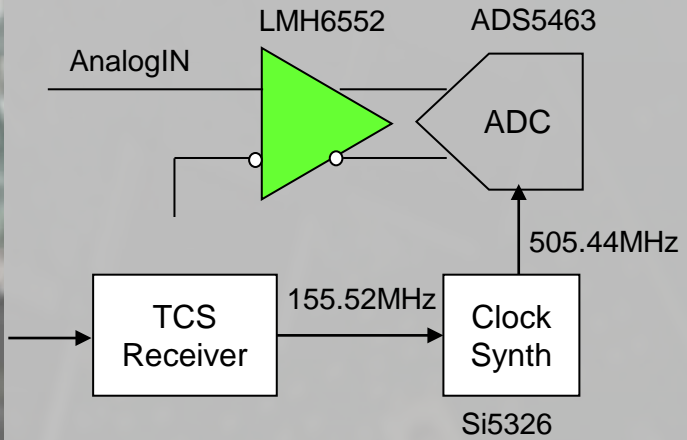


Jitter of sampling clock increases noise on signal and reduces Effective Number of Bits

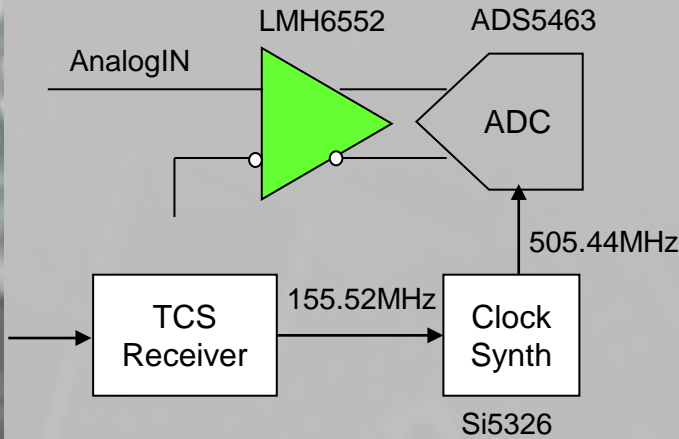
High Precision Clock Source needed!

$$\text{ENOB} = (\text{SNR} - 1.76) / 6.02$$

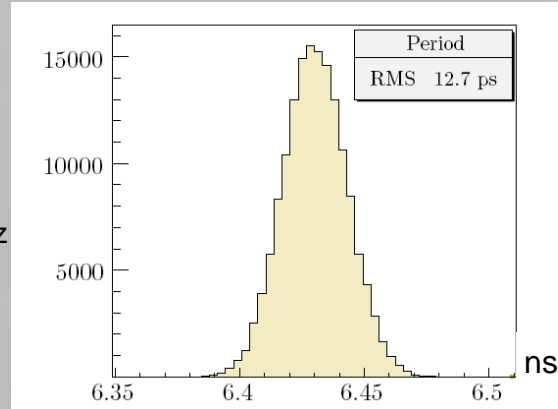
# Sampling Clock Quality



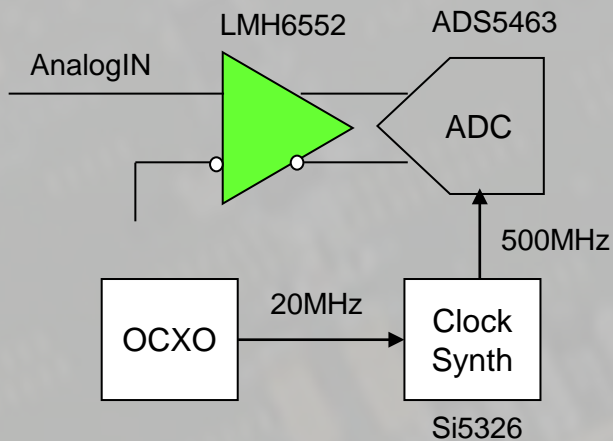
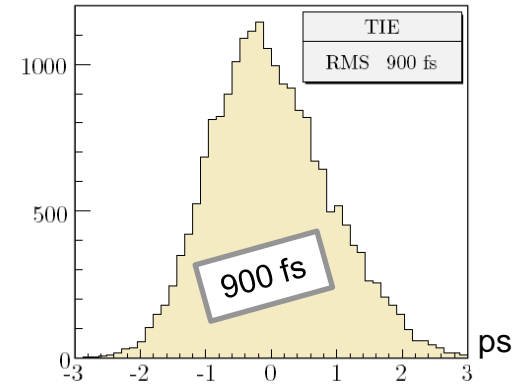
# Sampling Clock Quality



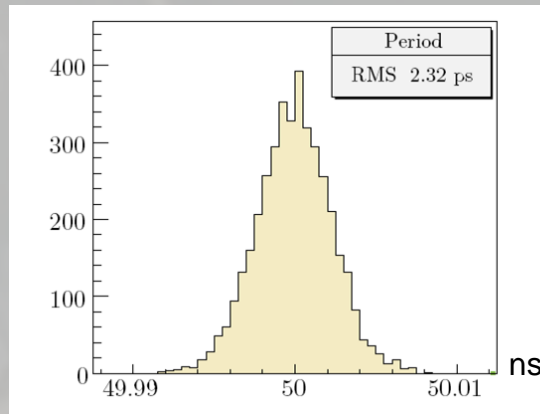
### TCS Jitter



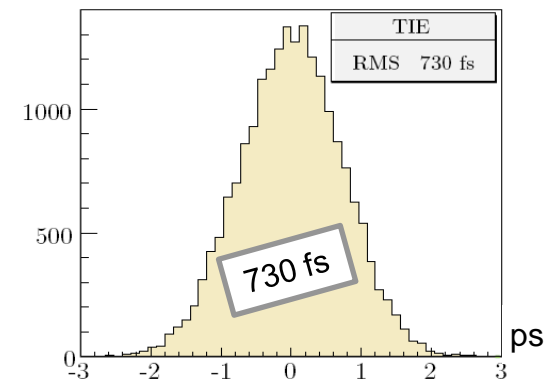
### Sampling Jitter



### OCXO Jitter



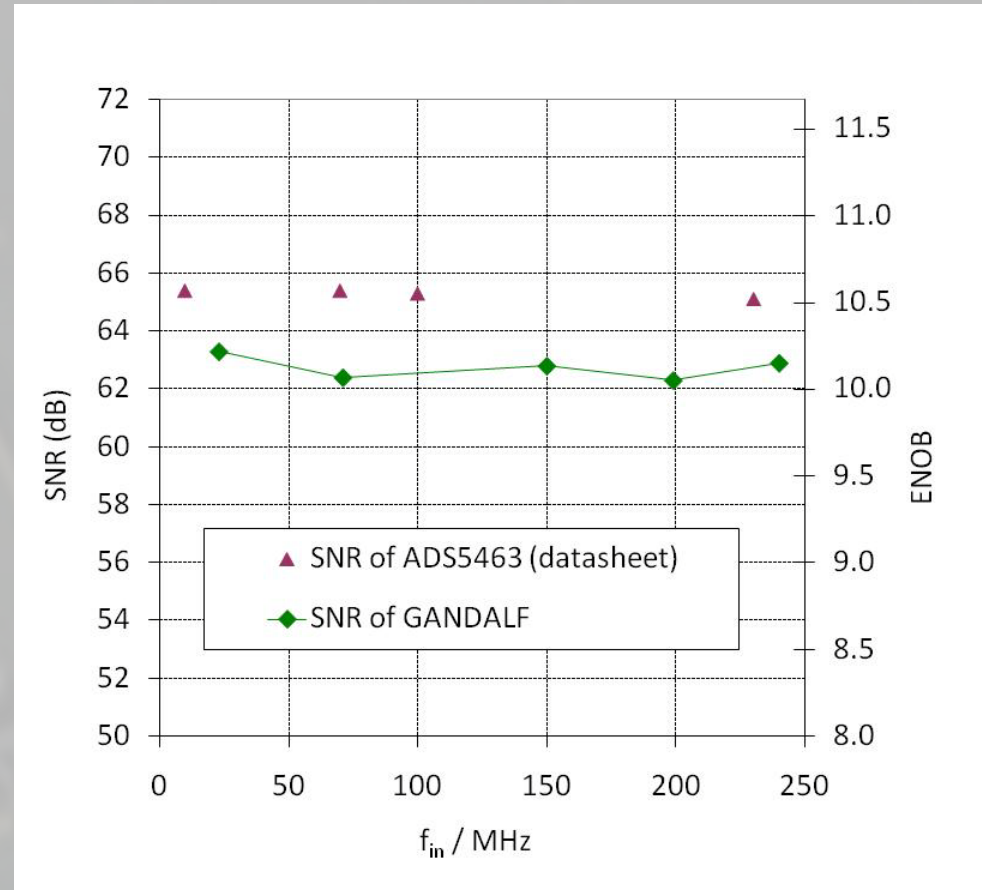
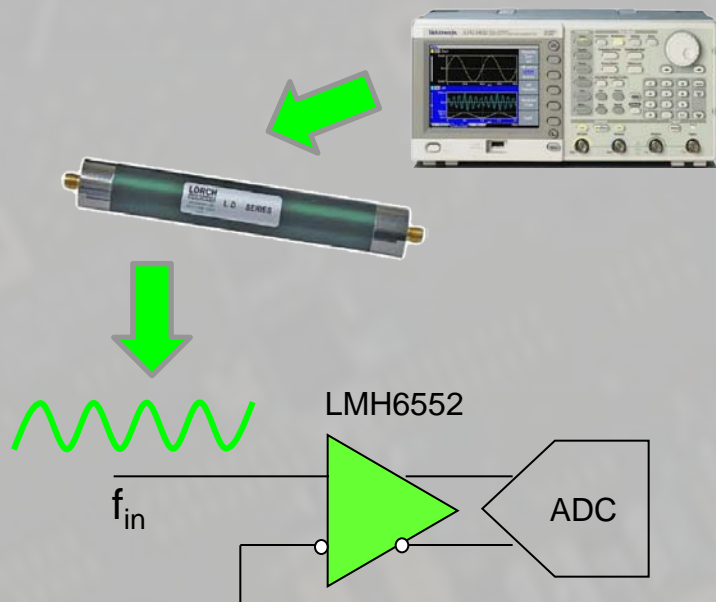
### Sampling Jitter



# GANDALF Performance

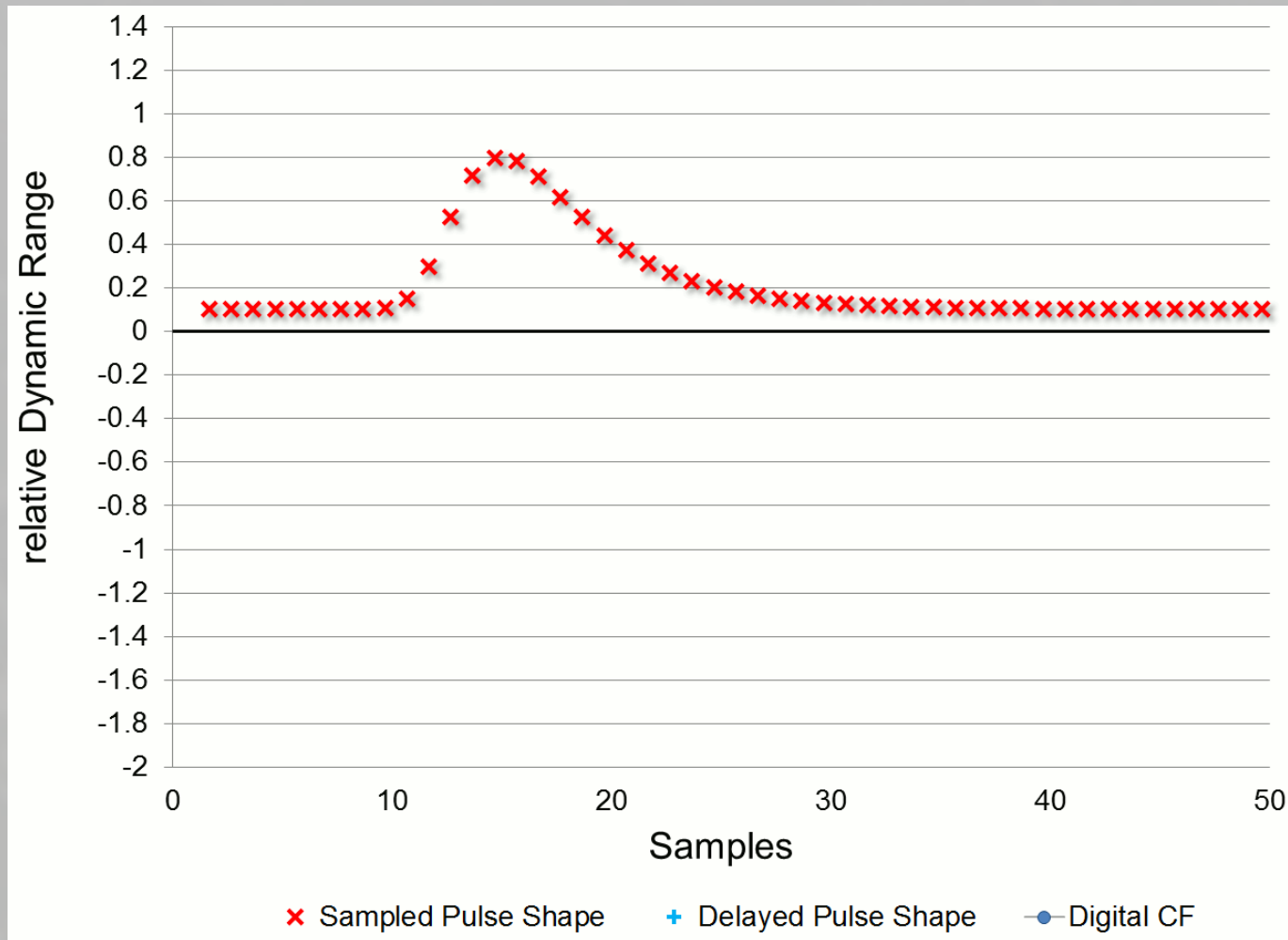
- Signal-to-Noise Ratio (Effective Number of Bits)

Measurement Setup:  
AFG3252 and  
high performance  
band-pass filters



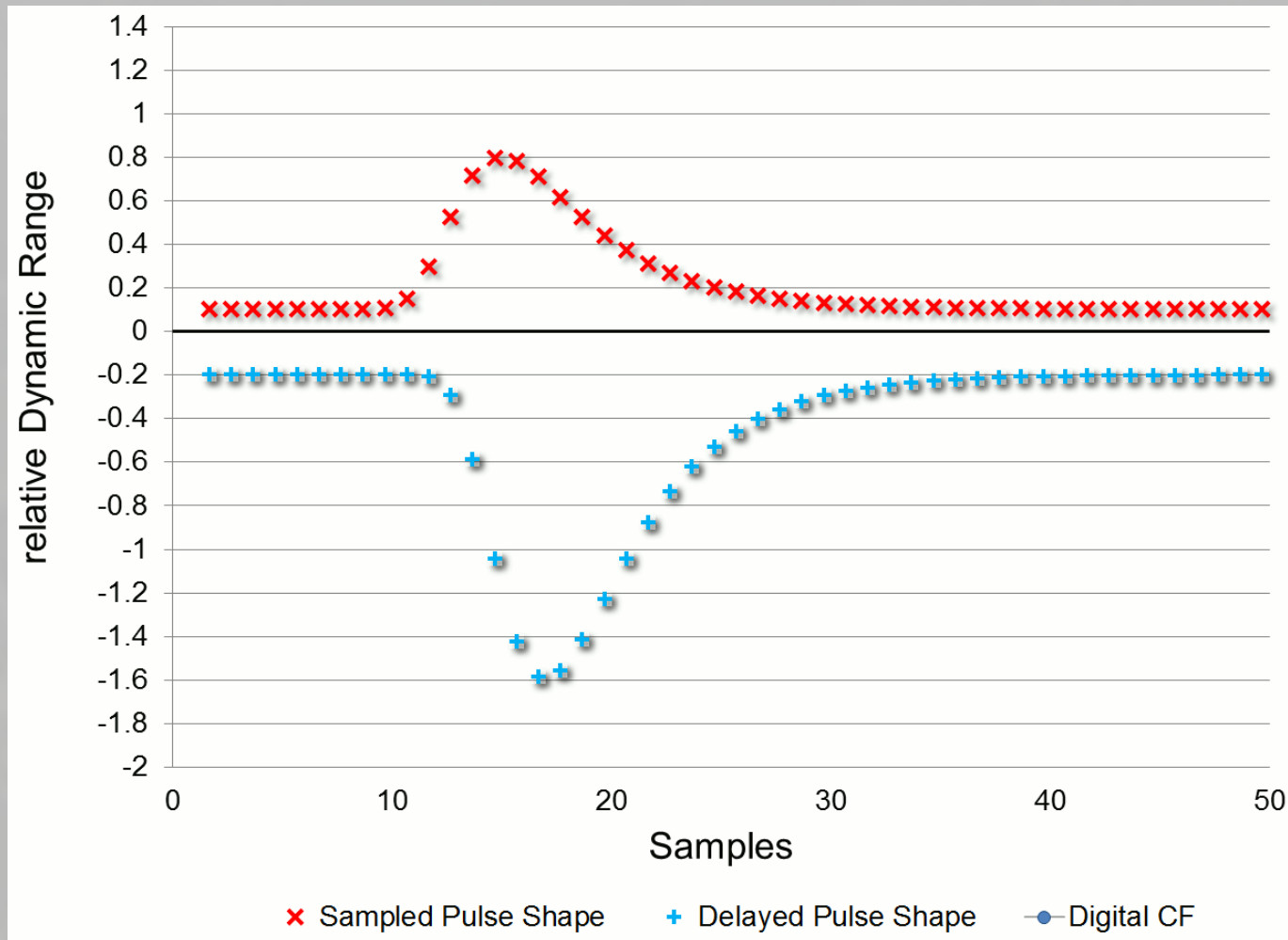
# Fit Algorithms for Time Extraction

- Digital Constant Fraction Discrimination



# Fit Algorithms for Time Extraction

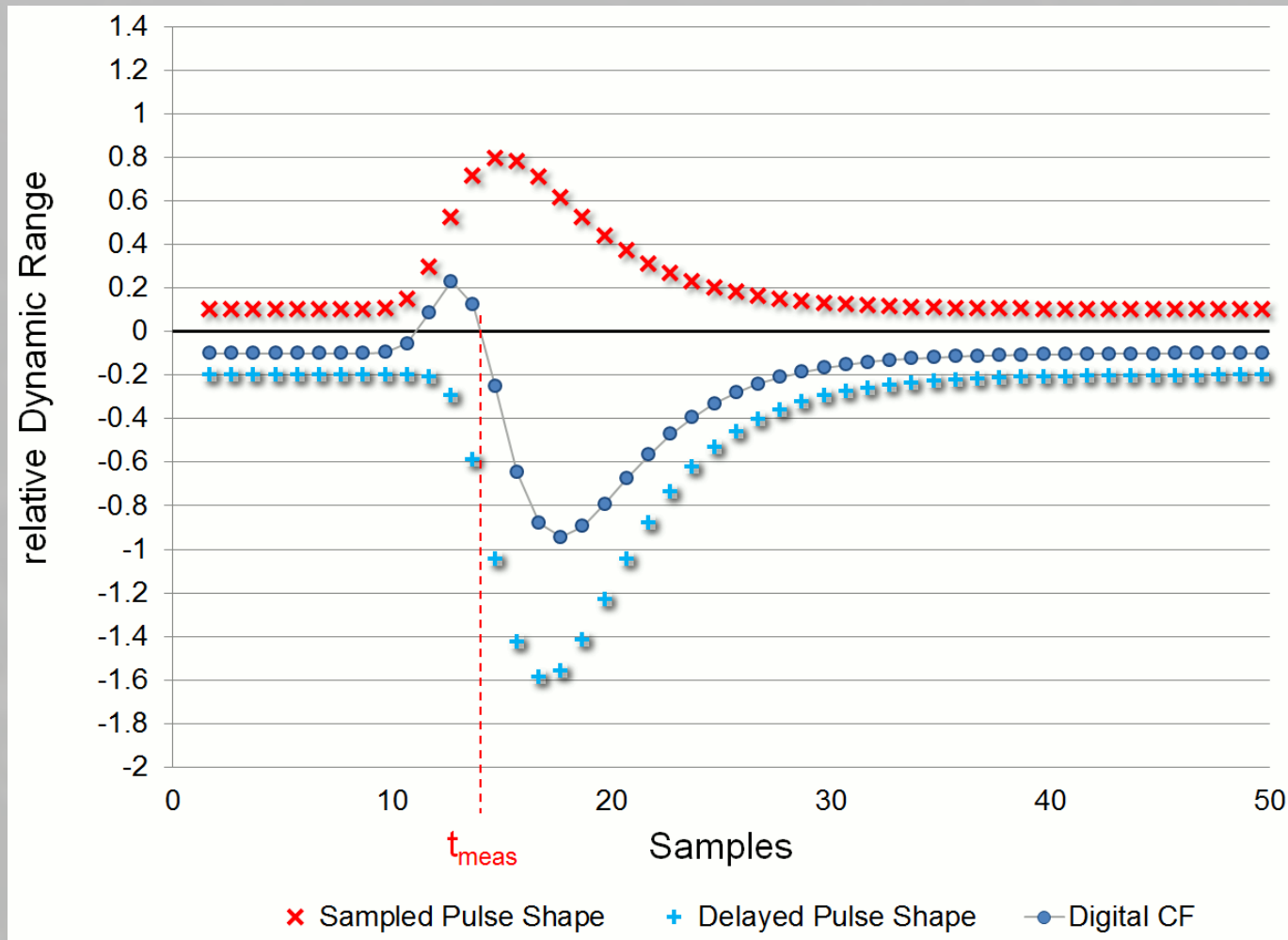
- Digital Constant Fraction Discrimination





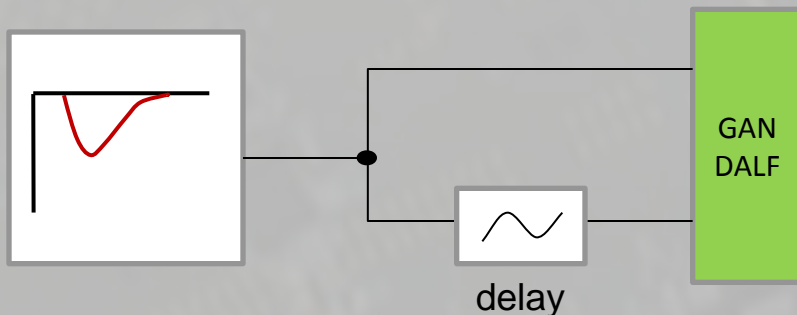
# Fit Algorithms for Time Extraction

- Digital Constant Fraction Discrimination

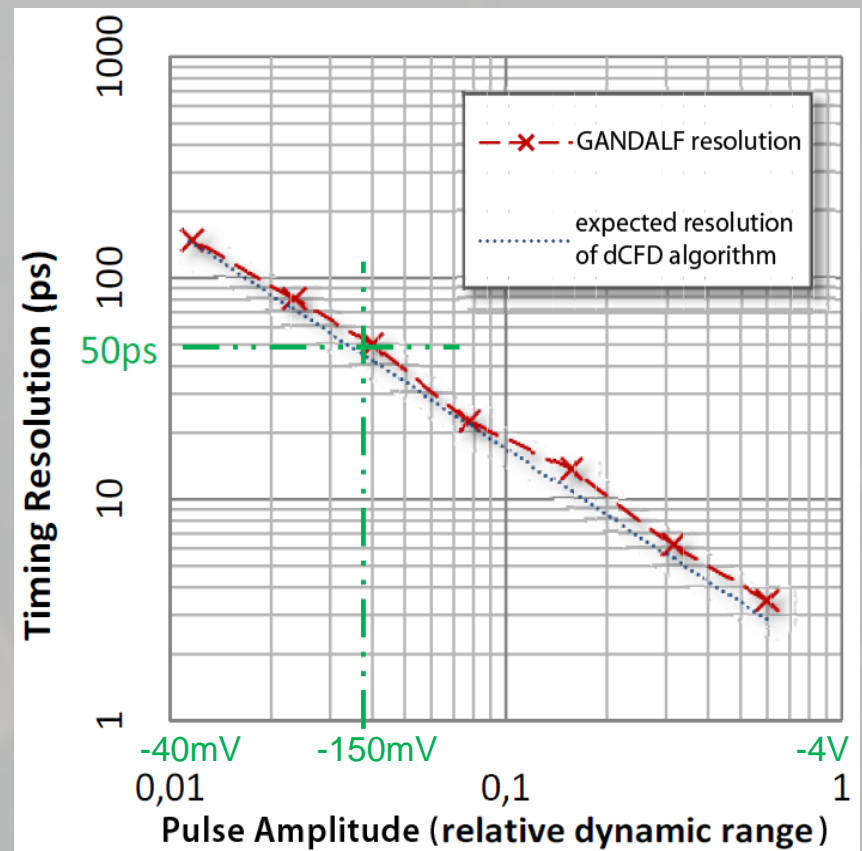


# GANDALF dCFD Performance

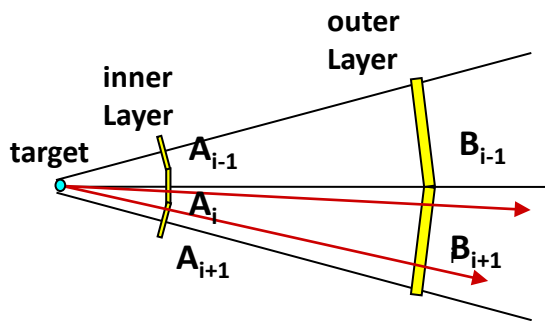
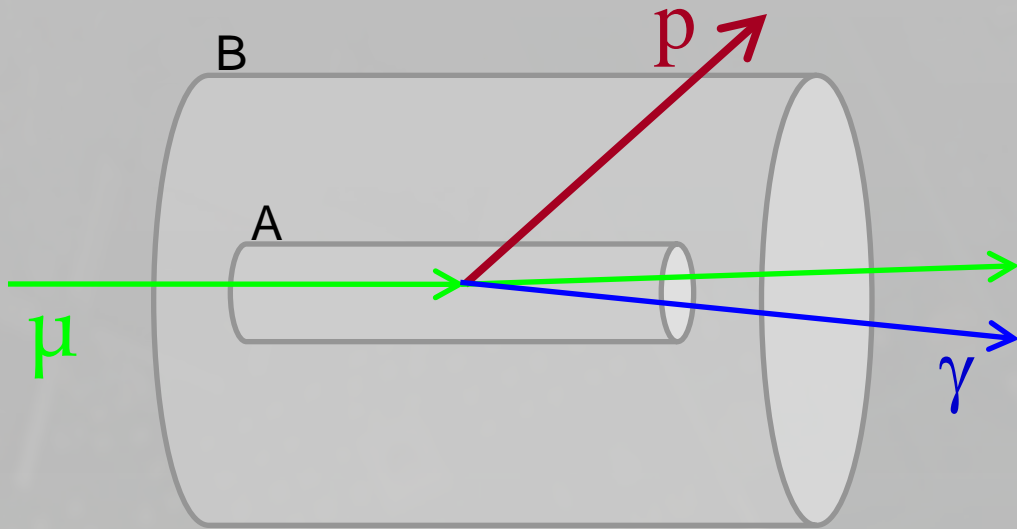
- created PMT-like pulses with function generator
- determined the time difference between delayed signals



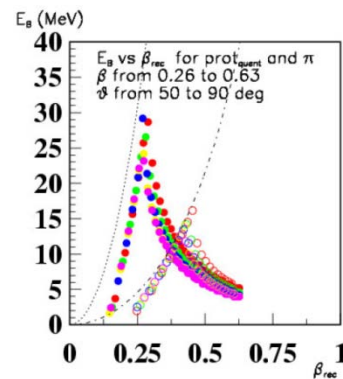
timing resolution vs. pulse amplitude  
sampled in 1GS/s mode



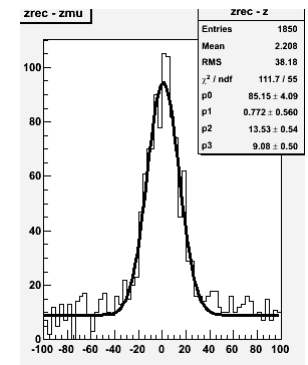
# Fast Recoil Detector Trigger



geometric structure



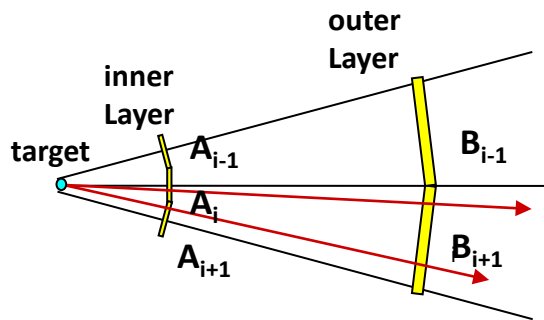
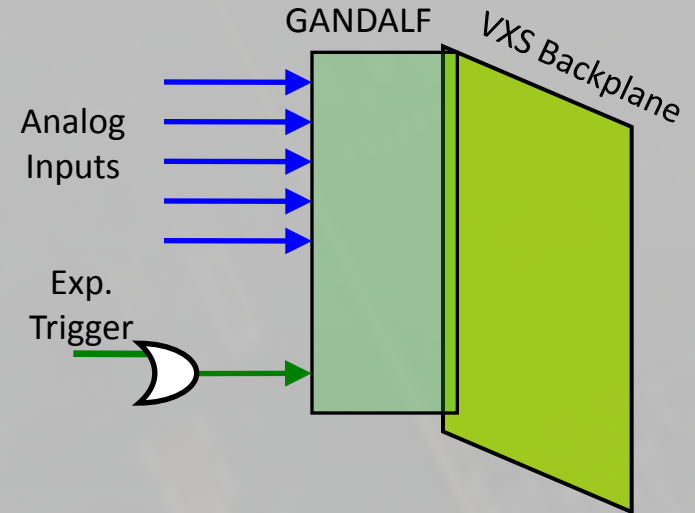
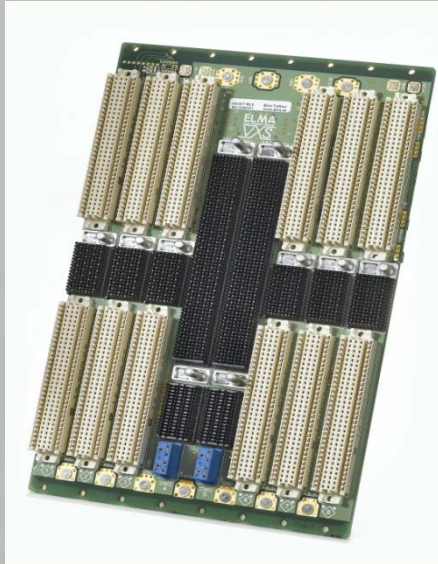
energy deposit vs.  $\beta$



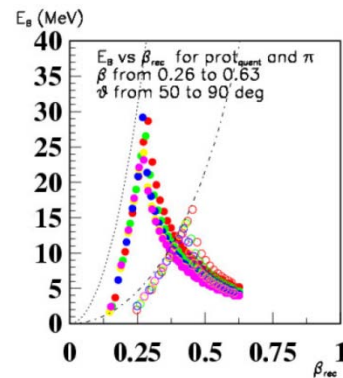
t proton - t muon

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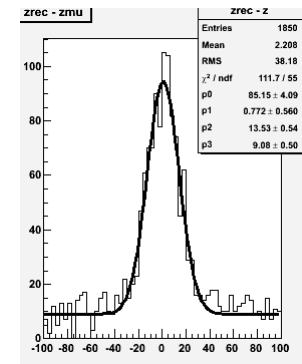
VITA 41.0  
Specification



geometric structure



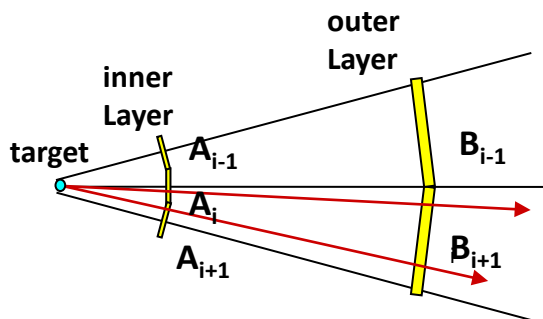
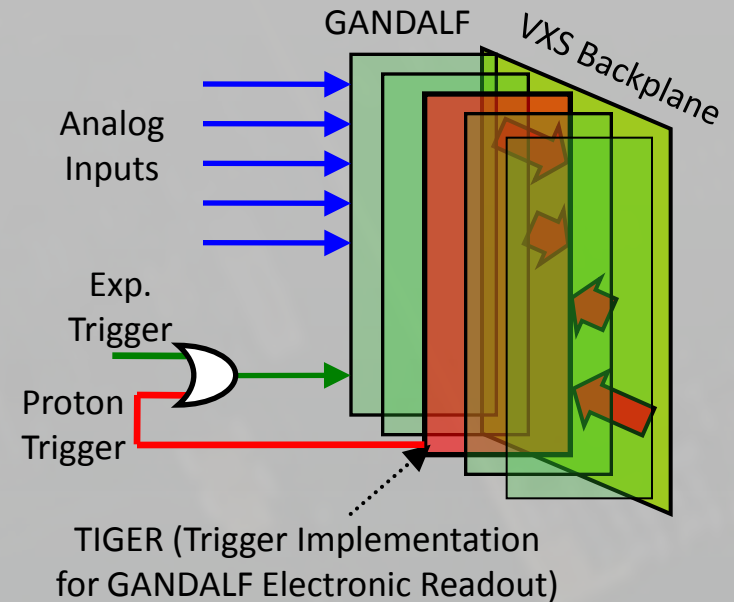
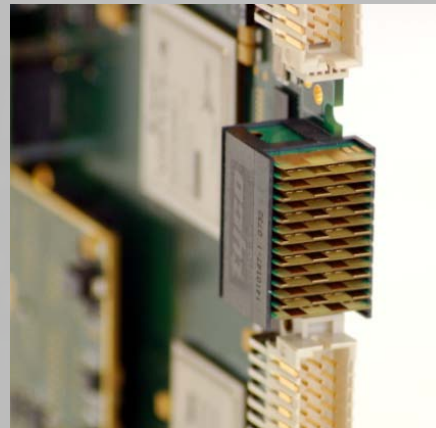
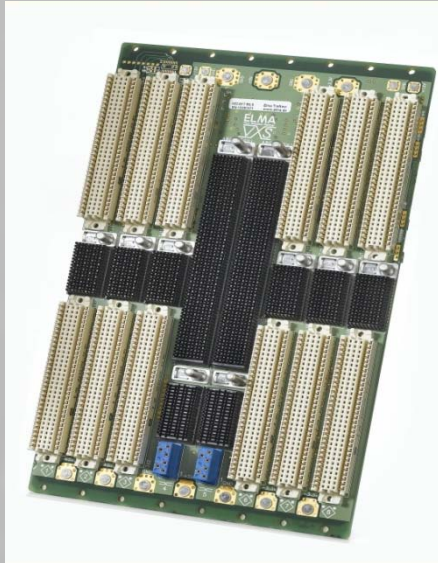
energy deposit vs.  $\beta$



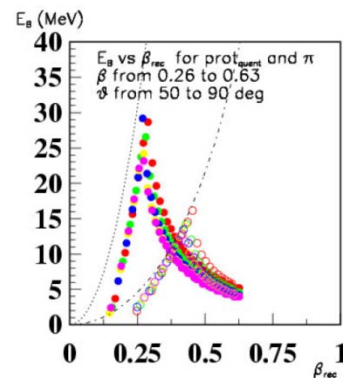
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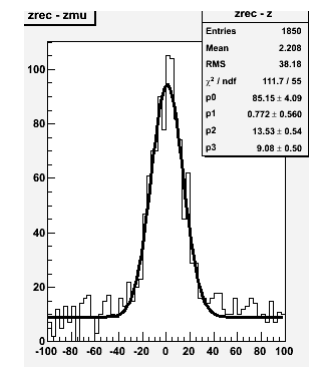
VITA 41.0  
Specification



geometric structure



energy deposit vs.  $\beta$



t proton - t muon

# Generic Advanced Numerical Device for Analog and Logic Functions

- ... is a VME64x readout system for nuclear and particle physics
- ... is a transient recorder which meets all design goals:
  - Effective Number of Bits > 10 bit
  - Time resolution < 50 ps
- ... is a VXS payload board to allow multi-module trigger decisions
- ... can also be equipped with digital inputs for other applications (cf. M. Büchele [HK 14.2] and J. Bieling [HK 14.4])

<http://hadron.physik.uni-freiburg.de/gandalf/>

