A multichannel Time-to-Digital Converter (TDC) inside a Virtex-5 FPGA on the GANDALF module

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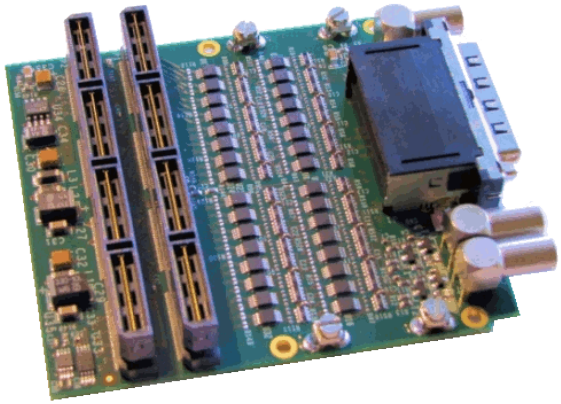
Overview

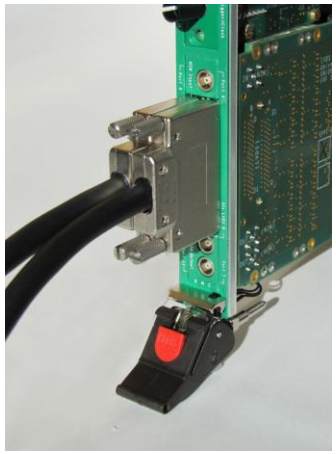
- GANDALF with Digital Mezzanine Cards
- TDC concepts
- TDC implementation in the FPGA
- measurements
- conclusion

Digital Mezzanine Card (DMC)



- 2 x 32-channel VHDCI connectors
- 64 differential inputs (LVDS and LVPECL) or

  64 differential outputs (LVDS)
- 1x NIM input, 2x NIM outputs
- jitter contribution < 25 ps



→ Multichannel TDC:

2x DMC per GANDALF module

=> 128 TDC channels

more about GANDALF module:
http://hadron.physik.uni-freiburg.de/gandalf/

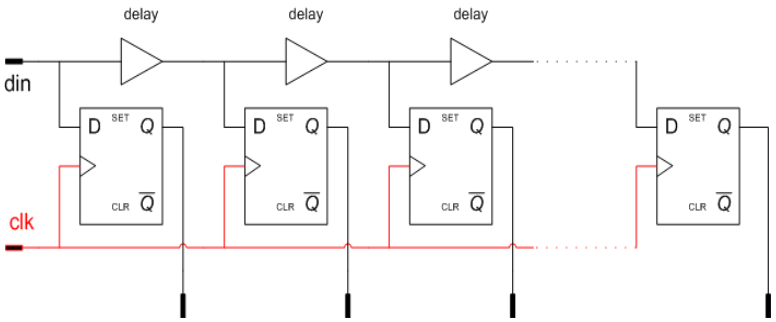
TDC concepts

Trivial concept of TDC

sampling of data signal → TDC bin width = $1/f_{max} \approx 2$ ns
f_{max} : 500 MHz (Virtex-5)

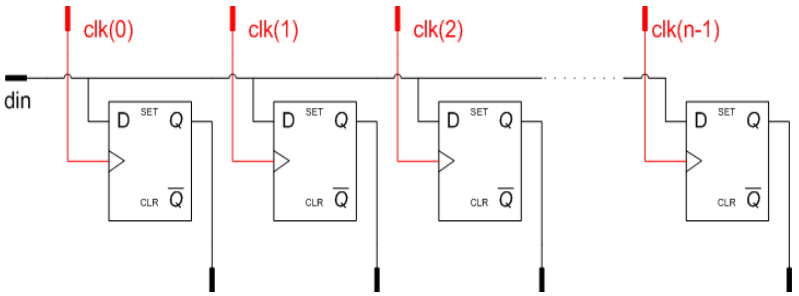
reduce TDC bin width by:

Delayed Data Sampling



- equidistant *delay* of data signal $\Delta t_{delay} = 1/(n*f_{clk})$
- same clock signal at flip-flops

Shifted Clock Sampling

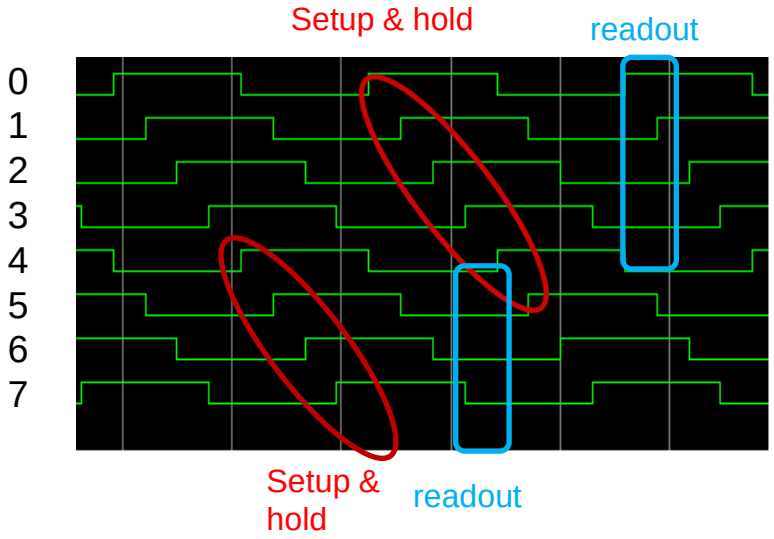


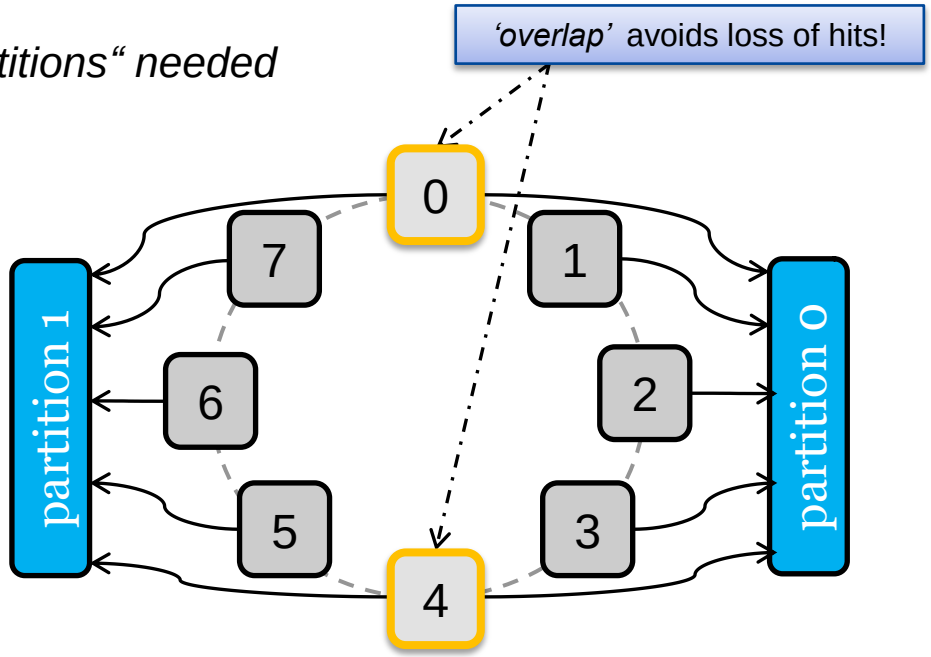
- equidistant *phase shift* of clock signal $\varphi_{delay} = 2\pi/n$
- same data signal at flip-flops

Partitions

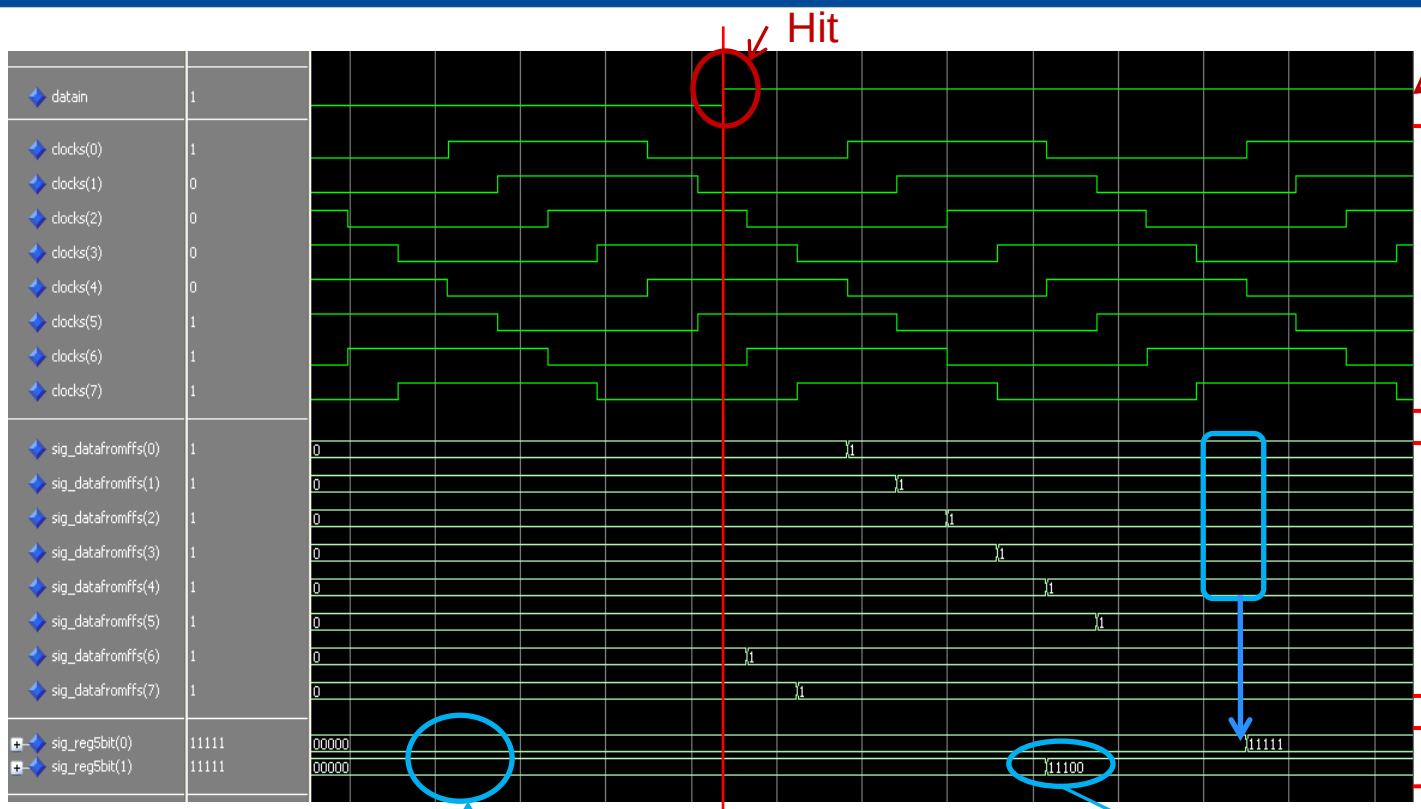
Shifted Clock Sampling:

- FPGA Clock Management Technology
  - *clock phase and frequency modulation with PLLs*
- different Clock Domains
  - *asynchronous register outputs => „partitions“ needed*





Readout example (VHDL simulation)



check for 'bit pattern' ≠ "00000" or "11111"

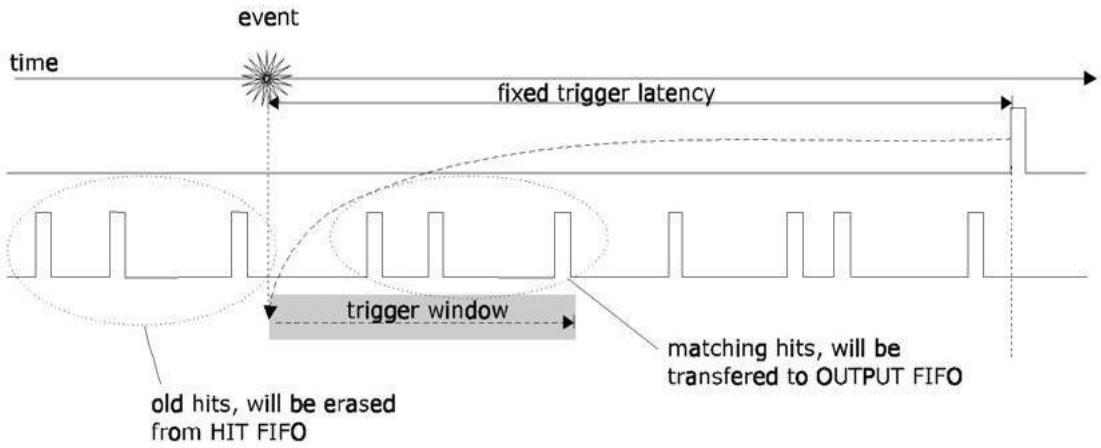
bit pattern "11100" → hit selected!

*time(TDC bin) = clk_counter * 8 + 'bitswap' position*

Trigger Matching

- time stamp measurements
- select only hits within a time window around a trigger signal
- trigger signal is related to data in the past

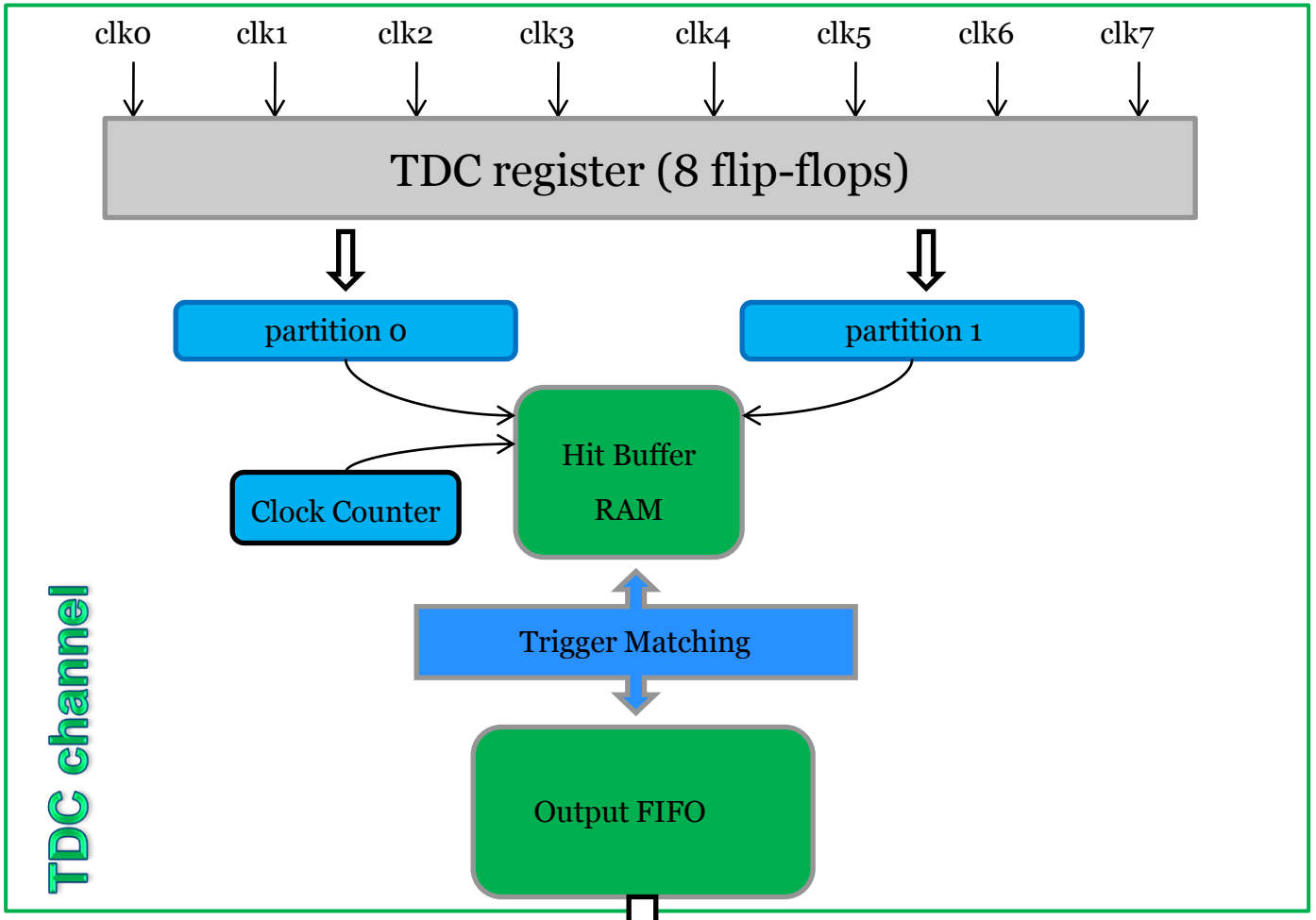
  → *hit data storage inside FPGA needed*



✓ max. latency: 20 µs

✓event FIFO depth: 1k

TDC overview



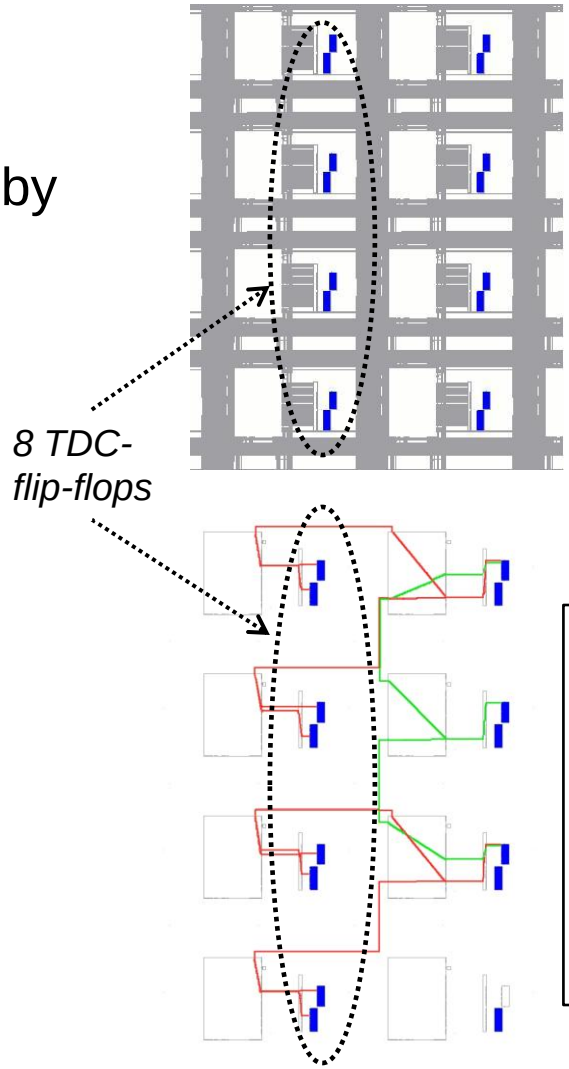
Implementation

Challenge

- accuracy of TDC bin width influenced by
  - → clock „jitter“
  - → clock „phase error“
  - → „routing delay“ of data signal

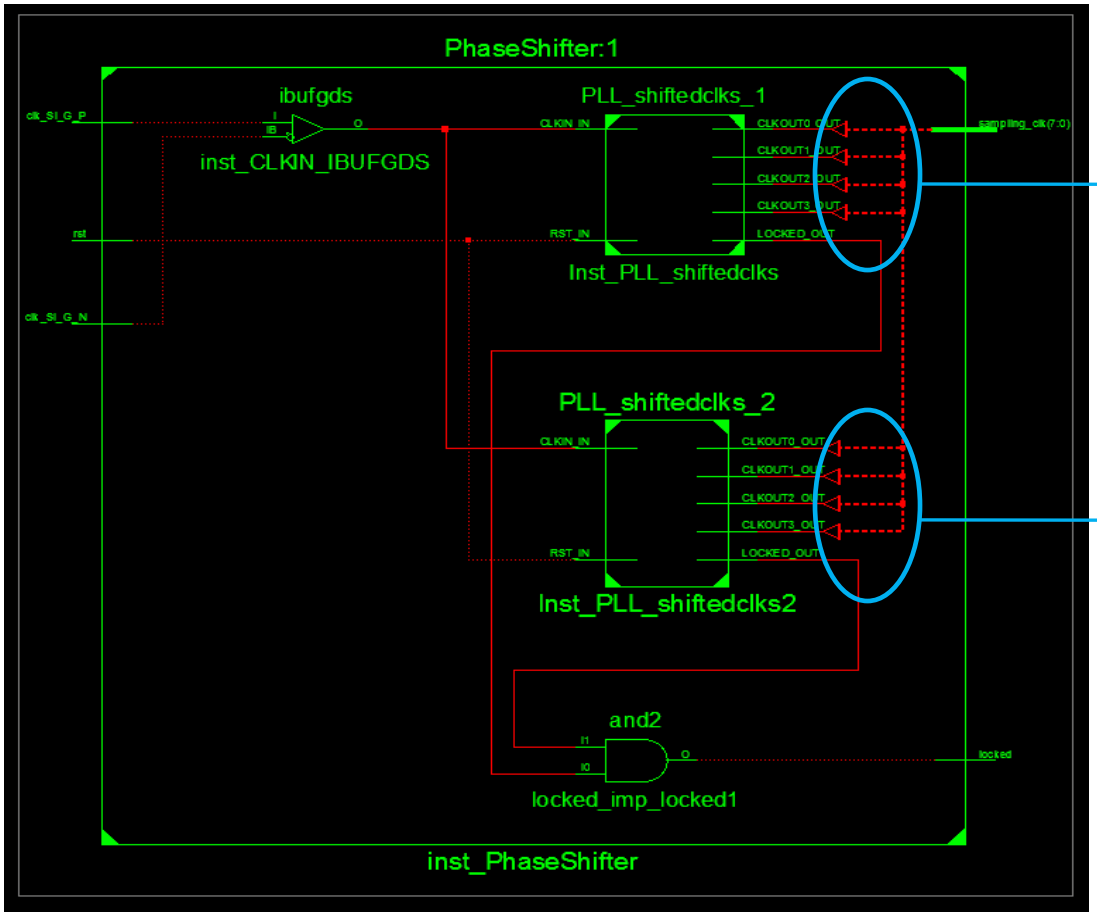
```
================================================================================
Timing constraint: NET "inst_TDC_8bin/sig_DatatoFFs_A" MAXSKEW = 0.025 ns;
 1 net analyzed, 0 failing nets detected.
 0 timing errors detected.
 Maximum net skew is    0.023ns.
--------------------------------------------------------------------------------
Slack:      0.002ns inst_TDC_8bin/sig_DatatoFFs_A
Report:     0.023ns skew meets    0.025ns timing constraint by 0.002ns
From                          To                          Delay(ns)  Skew(ns)
SLICE_X51Y91.D                SLICE_X48Y90.DX                0.284   0.023
SLICE_X51Y91.D                SLICE_X48Y91.DX                0.281   0.020
SLICE_X51Y91.D                SLICE_X49Y90.DX                0.284   0.023
SLICE_X51Y91.D                SLICE_X49Y91.CX                0.281   0.020

--------------------------------------------------------------------------------
```



Implementation

Phase-shifted clocks produced by PLLs



clock 0º
clock 90º
clock 180º
clock 270º

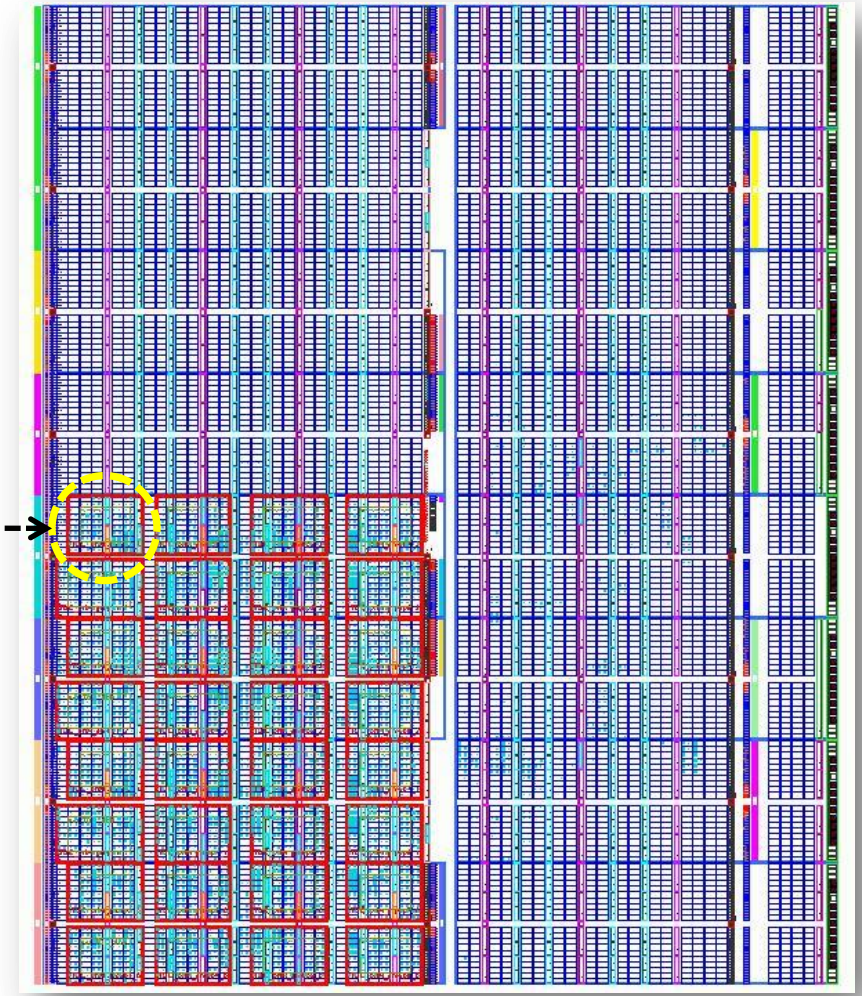
PLL 1

clock 45º
clock 135º
clock 225º
clock 315º

PLL 2

FPGA usage

- placement of 32 channels

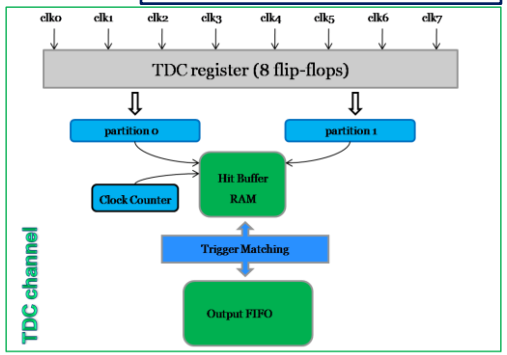


average resource usage per TDC channel

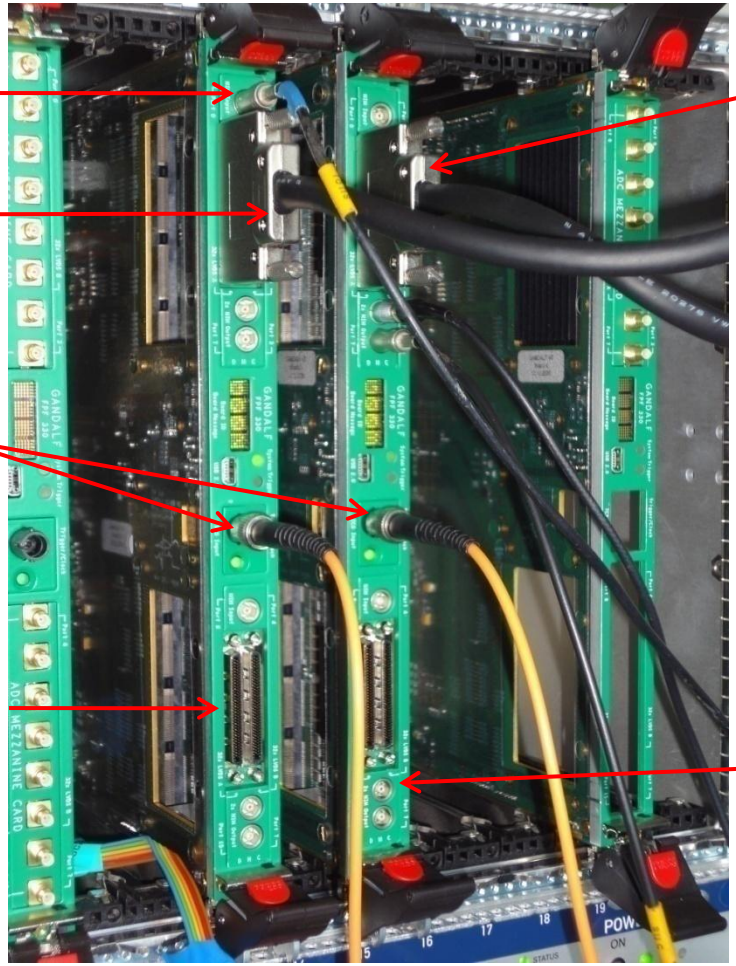
Physical Resource Estimates

Site Type	Available	Required	% Util
LUT	400	225	57
FD_LD	400	236	59
SLICEL	70	51	73
SLICEM	30	22	74
DSP48E	4	2	50
RAMBFIFO36	2	2	100
>RAMBFIFO36		1	
>RAMBFIFO18		1	
>RAMB18X2		1	

1 TDC channel



Measurements



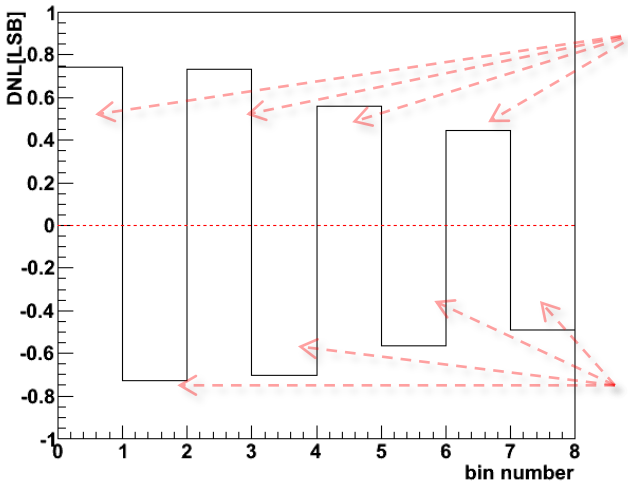
- 32 channels
- clock frequency 388.8 MHz
- 8 phase-shifted clocks

→ ***TDC bin: 320 ps***

Measurements

Differential Nonlinearity (channel 0)

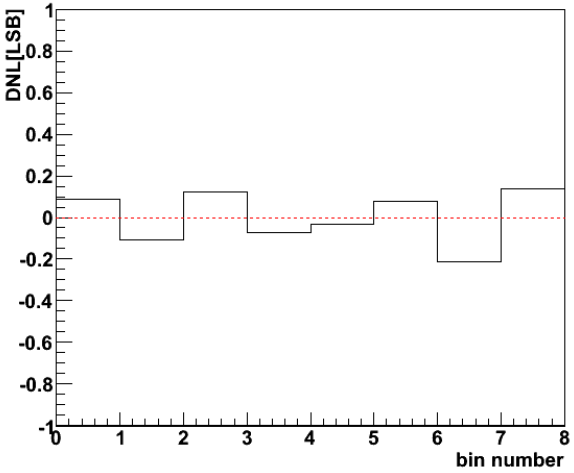
not optimized:

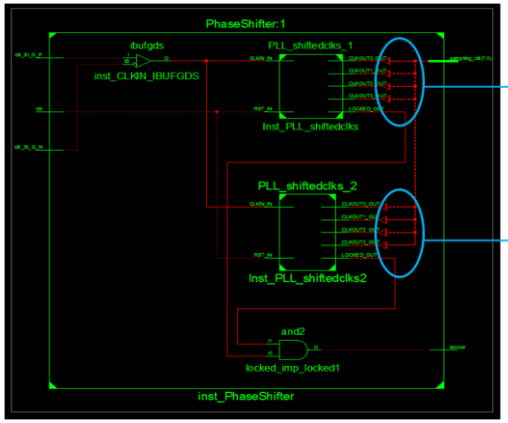


PLL1

PLL2

optimized:





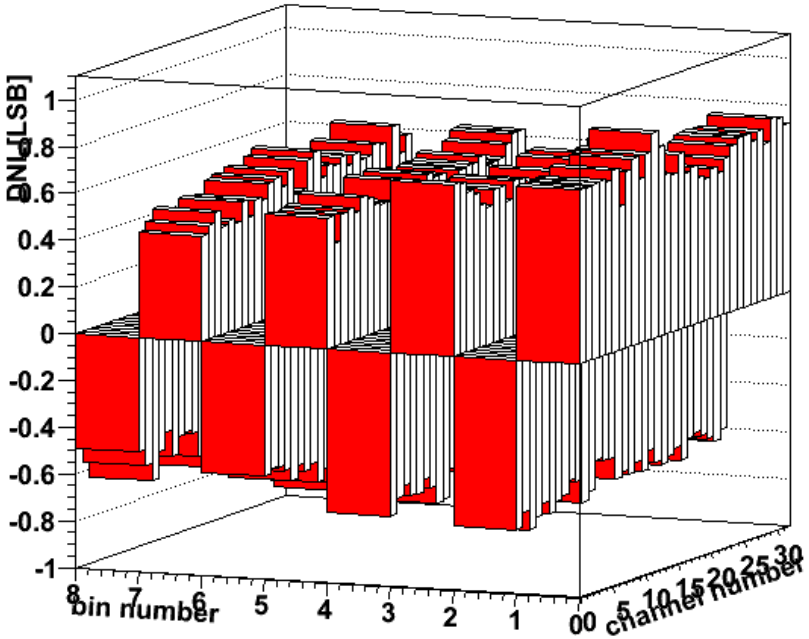
clock 0°
clock 90°
clock 180°
clock 270°
PLL 1

clock 45°
clock 135°
clock 225°
clock 315°
PLL 2

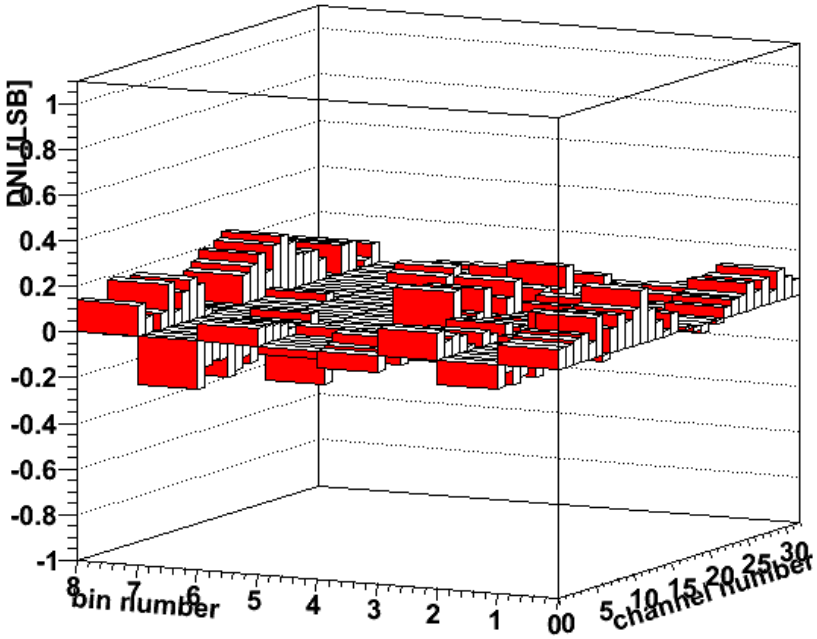
Measurements

Differential Nonlinearity (all channels)

not optimized:



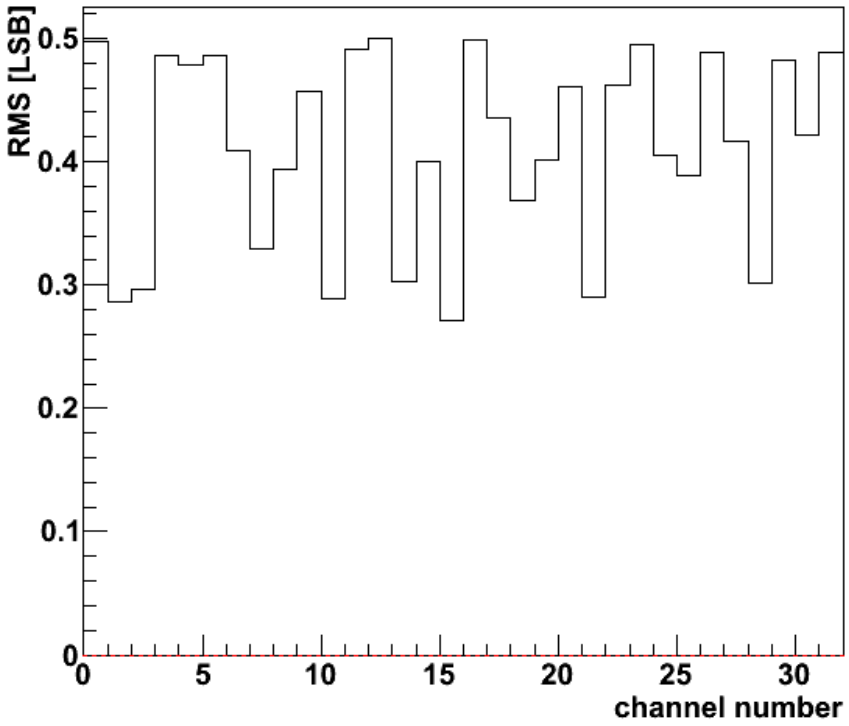
optimized:



Measurements

- time stamp difference '*channel x*' to the mean of all other channels:

TDC time resolution:
0.5 *LSB = 160 ps



Conclusion

presently:

- 32 TDC channels
- time resolution 160 ps

under progress:

- FPGA-design extension to **128 channels**
- bisection of TDC bin width can be achieved by locally inverting the clocks to produce 16 phase-shifted clocks → **TDC bin: 160 ps**