Der GANDALF 128-Kanal Time-to-Digital Converter (TDC)

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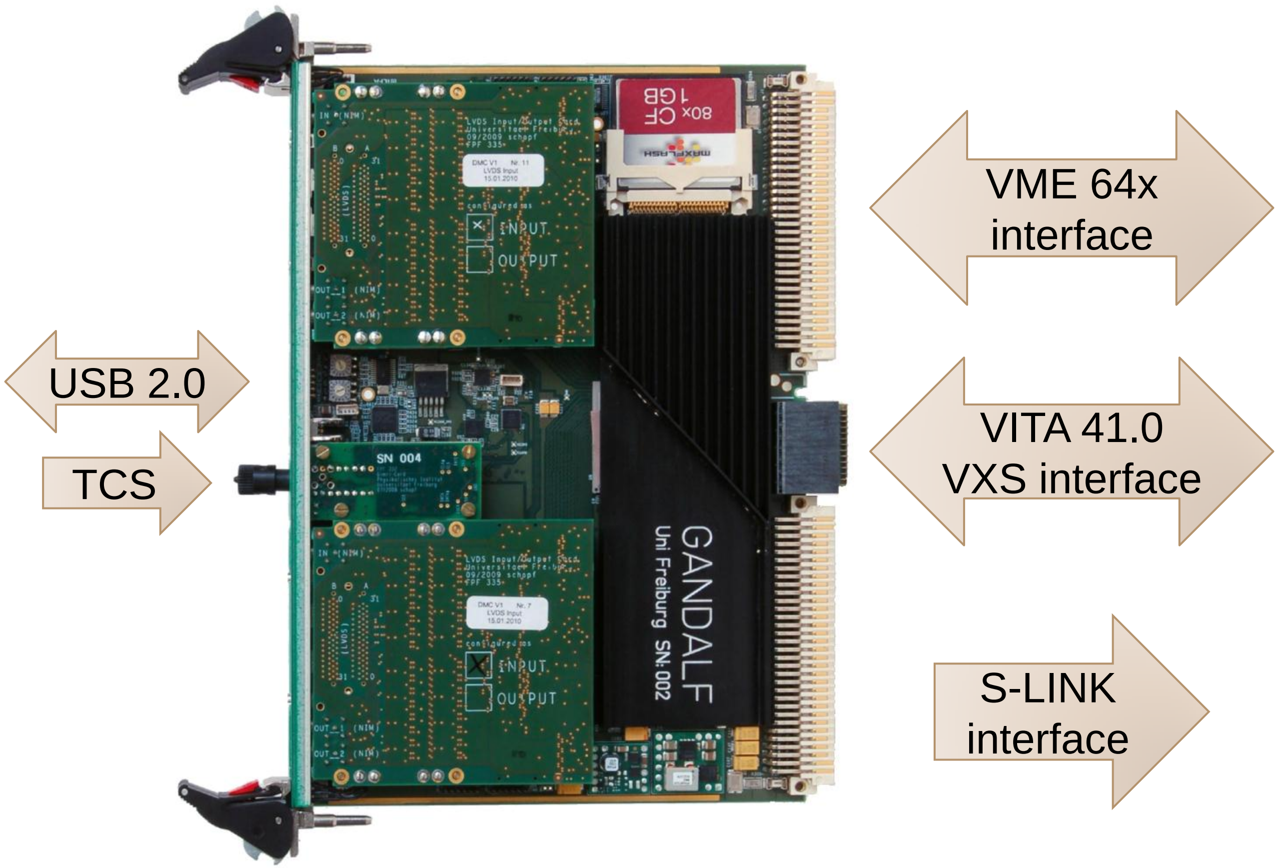
HK34.5, DPG Frühjahrstagung 2012, Mainz

UNI FREIBURG

bmb+f - Förderschwerpunkt
COMPASS
Großgeräte der physikalischen Grundlagenforschung

SEVENTH FRAMEWORK PROGRAMME

The GANDALF module



Virtex-5 SX95T FPGA
for Data Processing:

- *14720 Virtex-5 Slice*
- *8.7 Mbit Block RAM*
- *640 DSP48E Slice*

Virtex-5 LX30T FPGA
for Memory Control & Data Output:

- *4800 Virtex-5 Slice*
- *1.2 Mbit Block RAM*

Memory:

- *144 Mbit QDRII+*
- *4 Gbit DDR2*

Aurora Bus:

- *25 Gbit/s high speed FPGA interface*

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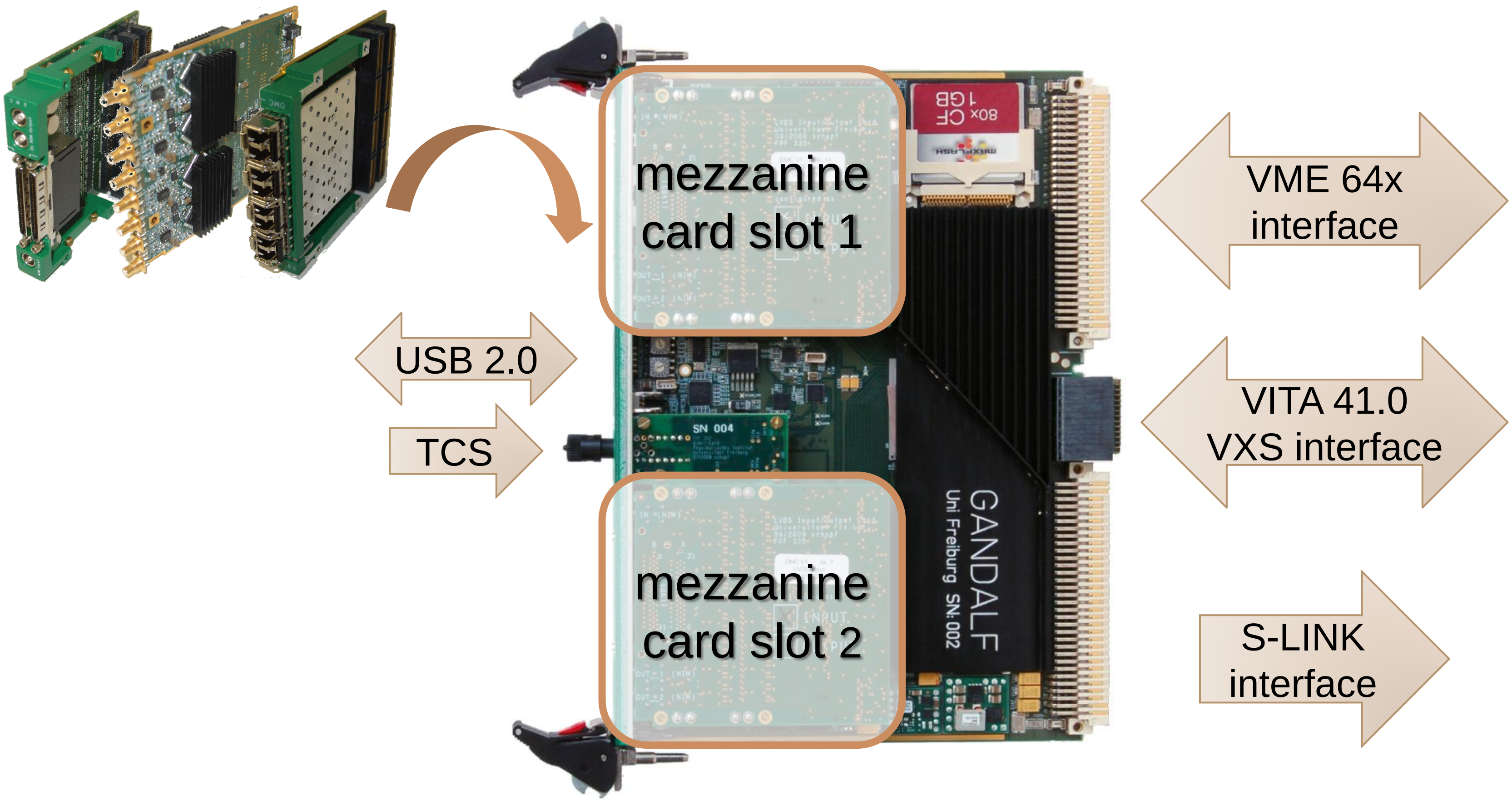

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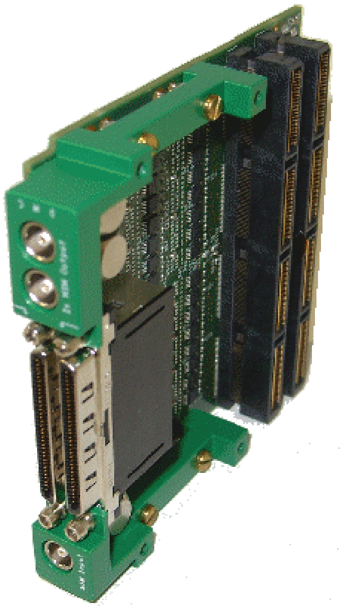
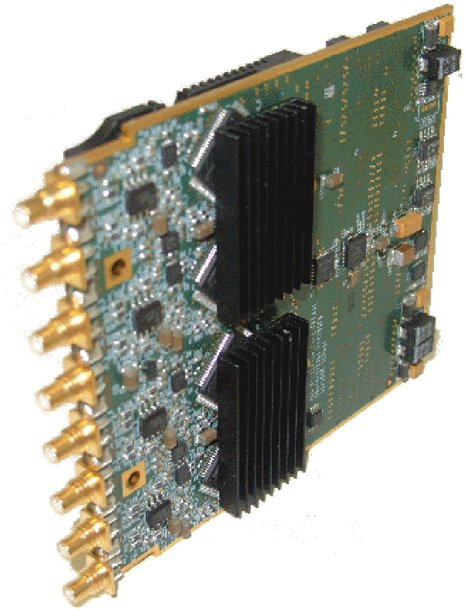
Mezzanine Cards



GANDALF with digital mezzanine cards

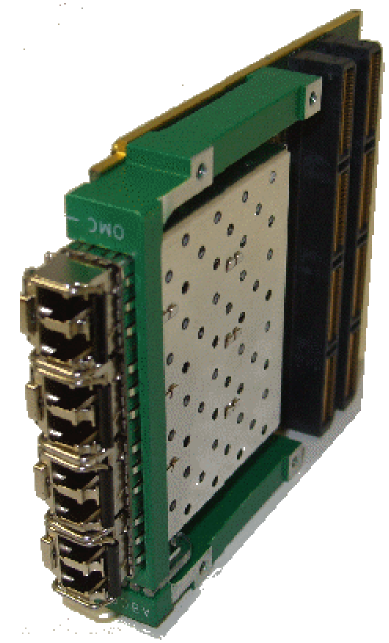
- 128 differential inputs or outputs
- Versatile I/O applications :

→ e.g. ***time-to-digital converter*** scaler, mean-timer, trigger logic



GANDALF transient recorder

- 16 analog inputs for A/D conversion *(500 MS/s @ 12 bit)*
- Real-time pulse shape analysis *(time resolution up to 10 ps)*
- ***See HK 35.6***



GANDALF with optical mezzanine cards

- 8 optical inputs or outputs
- High Speed Data Transfer to/from detector FE modules *(3.125 Gbit/s per channel)*

GANDALF TDC design objectives

- Implement 128 TDC channels in Virtex-5 FPGA

TDC specifications:

- Time resolution < 100 ps for time stamp measurements
- Leading and/or trailing edge sensitive
- Multi-hit capability
- 10 ns double hit resolution
- 16 bit dynamic range

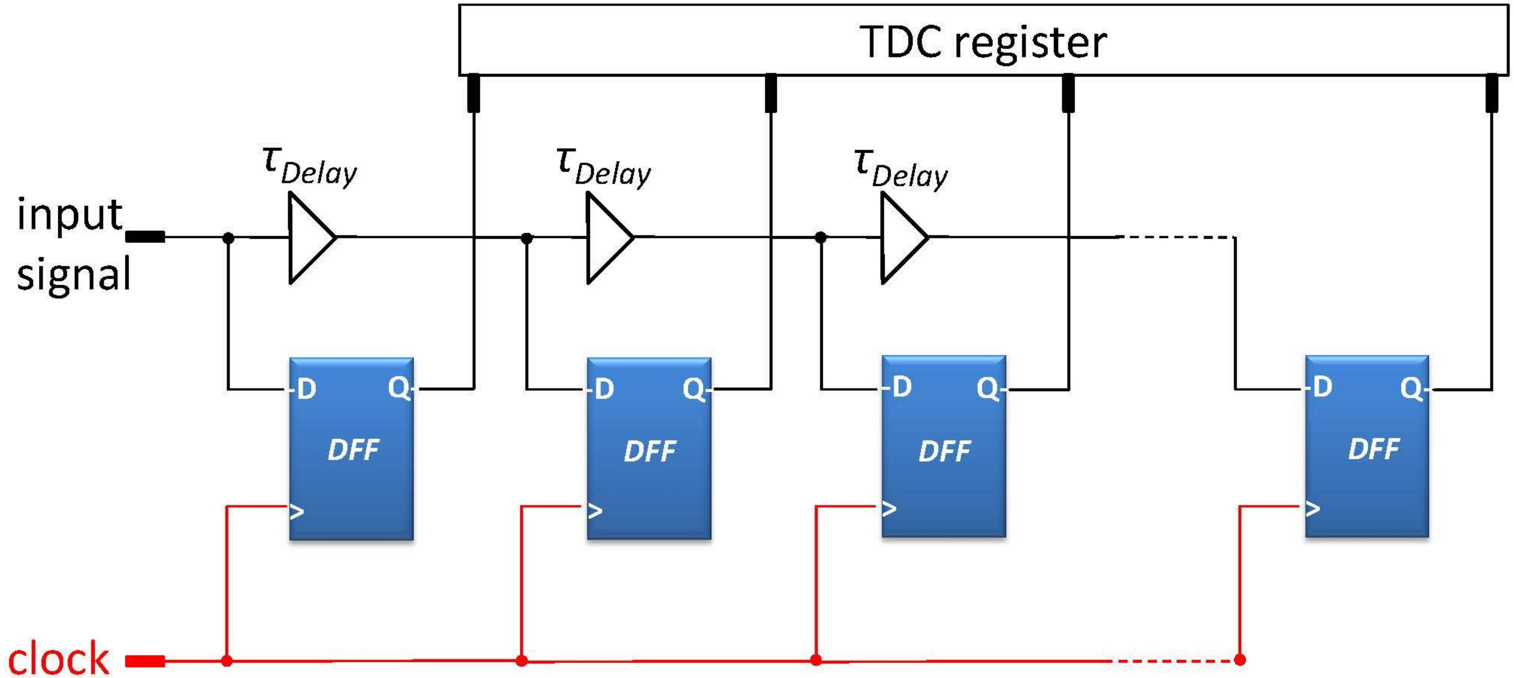
Advanced readout capability:

- 20 µs look-ahead/look-back hit buffer
- Programmable trigger window
- Dead-time free data readout

- Replace F1-TDC at COMPASS experiment

Time-to-Digital Converter

Common TDC concept:



Uniform propagation delays in FPGA is not trivial:

- e.g. carry chain $\sim 30\ ps$ *(Virtex-5)*

  + *High resolution TDC*

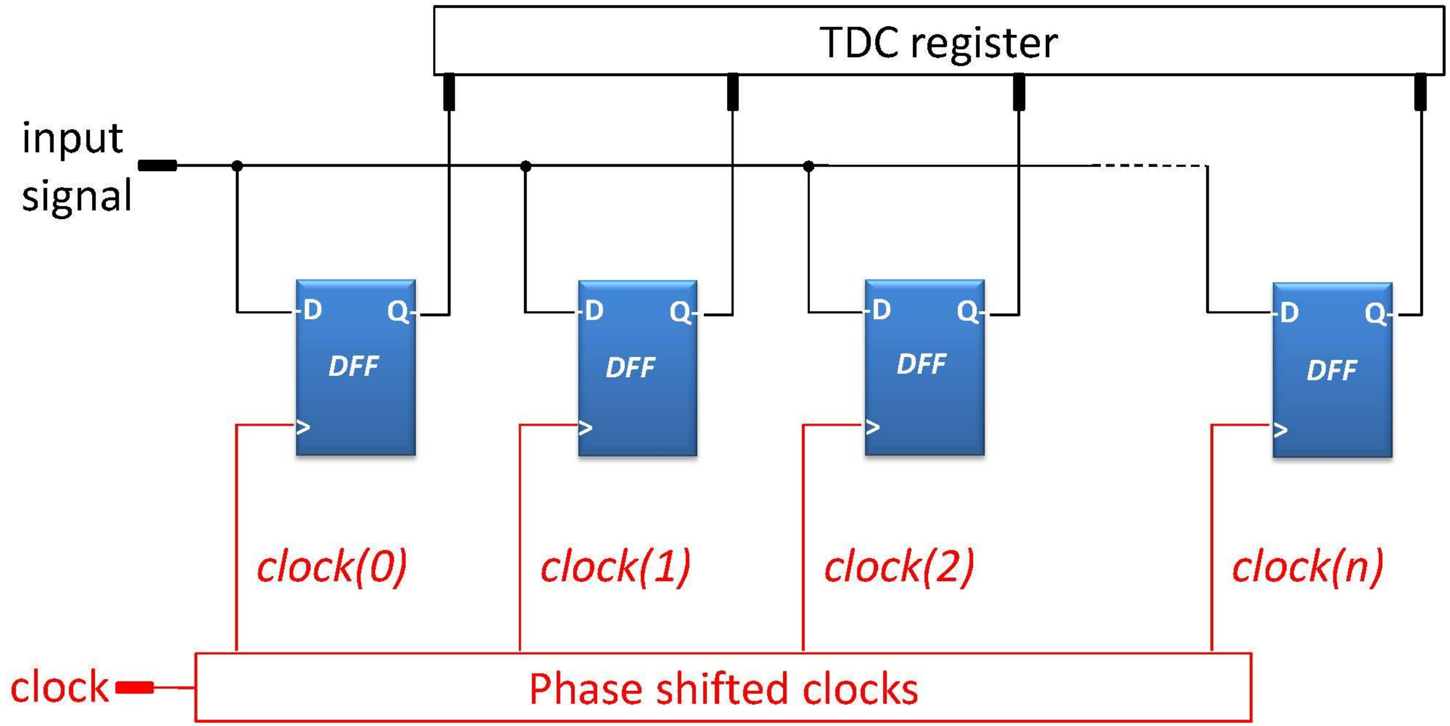
  - *Logic consumption exceeds device resources*

Delayed Data Sampling:

- $T_{clk} = n \times \tau_{Delay}$

Time-to-Digital Converter

Alternative TDC concept:

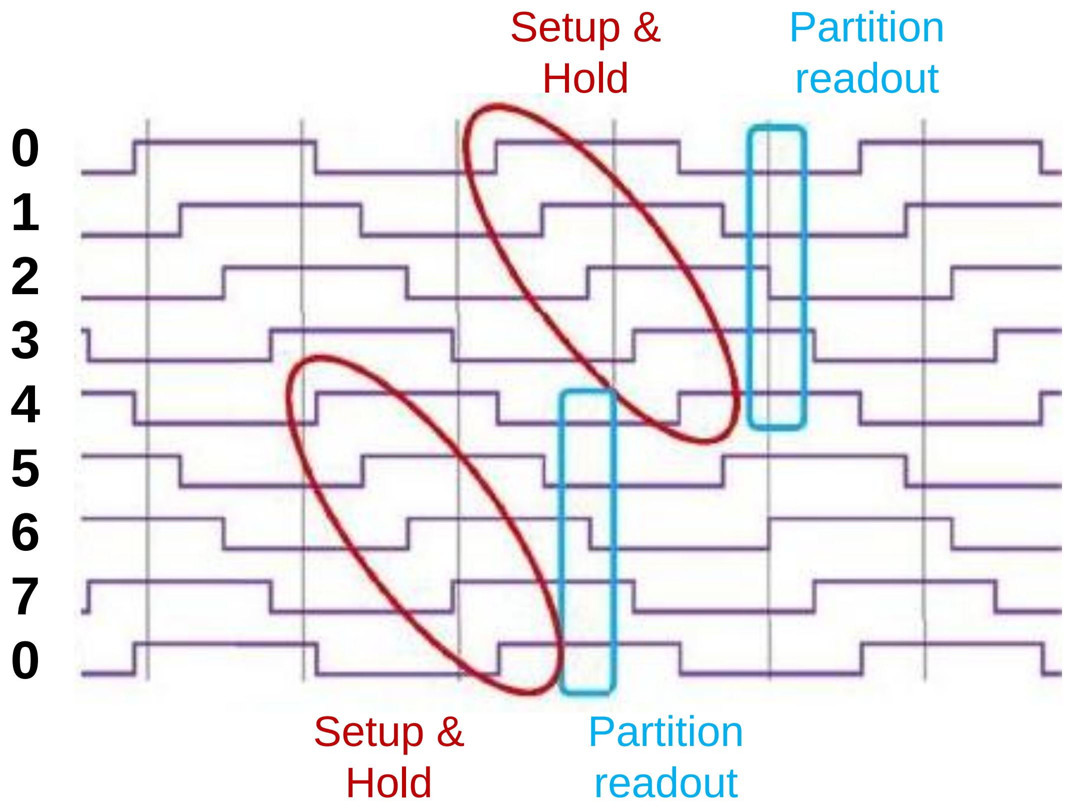


Shifted Clock Sampling:

- $360° = n \times \Delta\varphi$
- $time\ stamp = course\ counter + register\ output$

Time-to-Digital Converter

Alternative TDC concept:

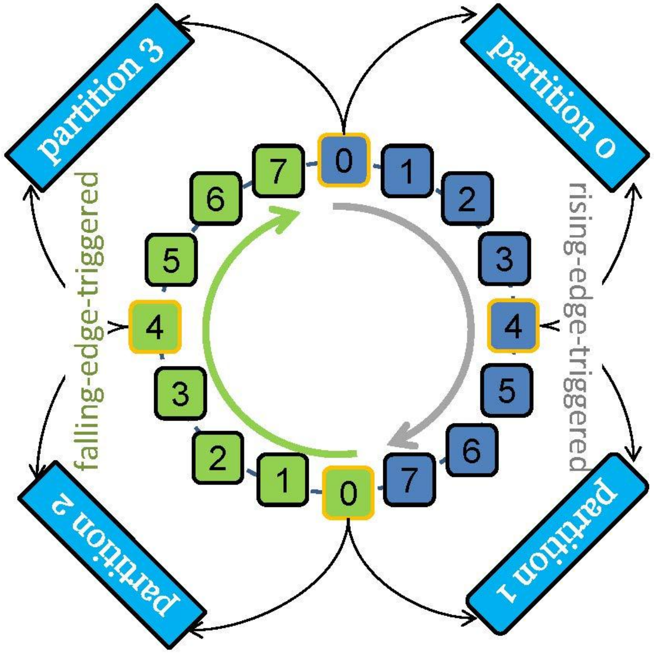


→ Synchronization of clock domains!

16-bin TDC design

- 16 phase-shifted clocks
- 8 clocks by 2 PLLs within FPGA

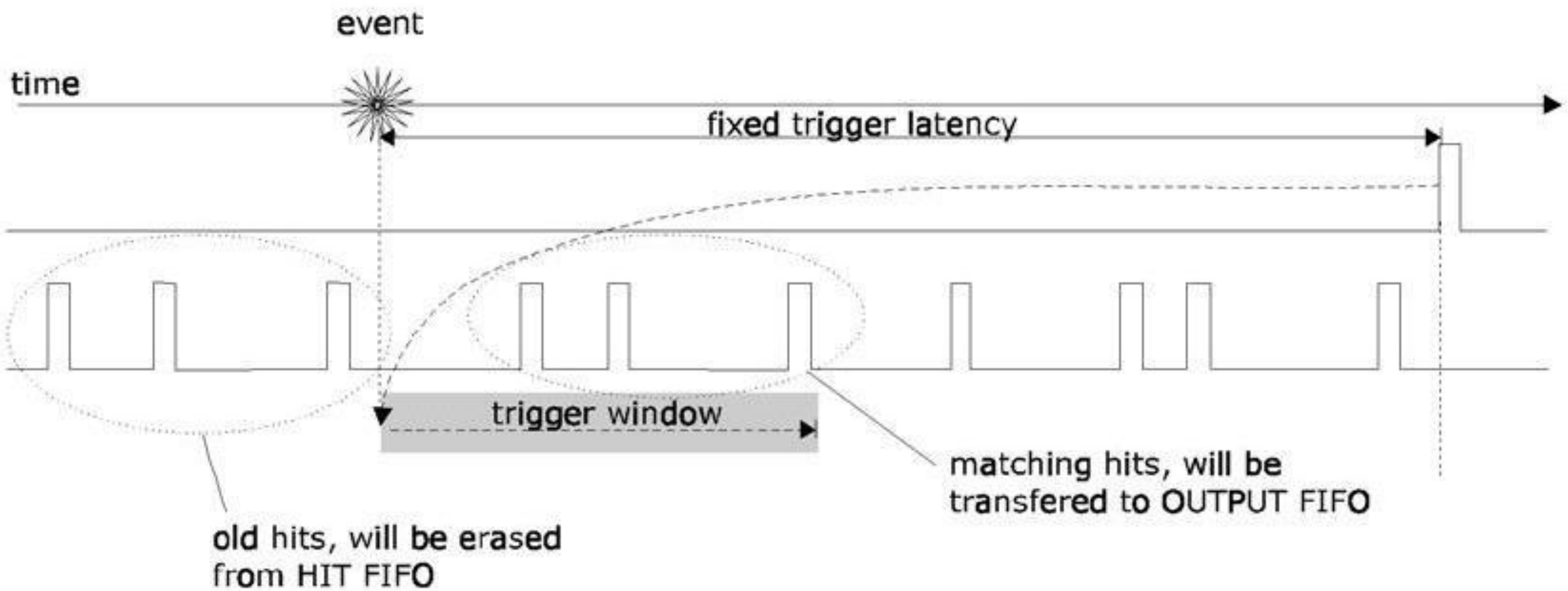
  8 more clocks by locally inverting clock signal
- TDC bin size: $\frac{1/_{388.8\,MHz}}{16} \approx 160\,ps$



(= *Flip-flop*)

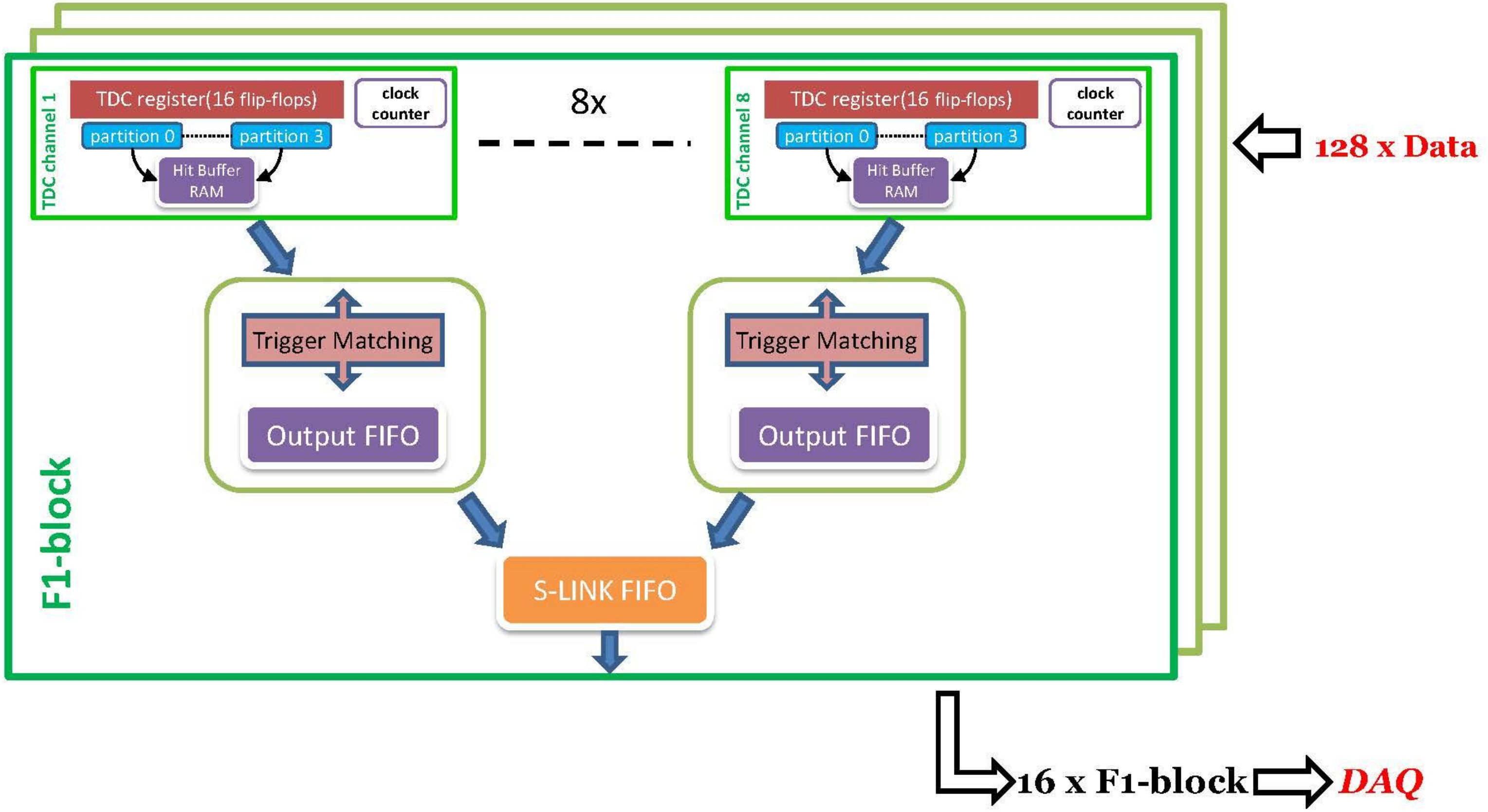
16-bin TDC design

- Trigger signal is related to data in the past:
  - → Data storage in FPGA needed (“*Virtex-5 Block RAM*”)
    - ✓ *memory depth 1k*
    - ✓ *max. latency 20 µs*



16-bin TDC design

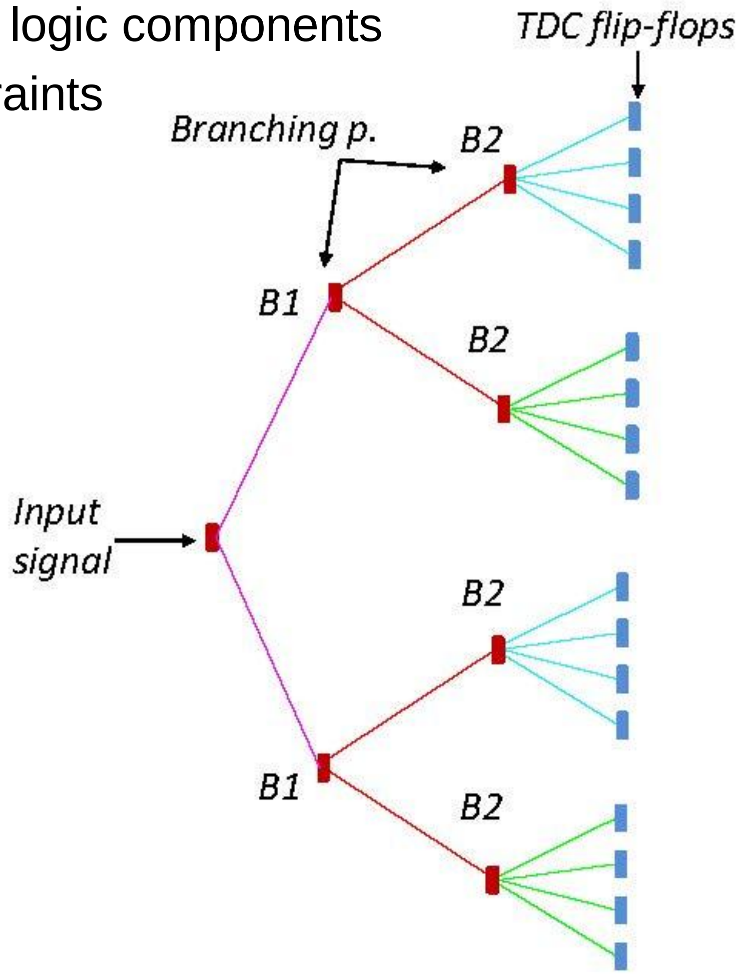
- F1-blocks combining 8 TDC channels:



FPGA implementation

Input signal routing skew:

- Branching points *("Virtex-5 Slice")*
- Placement of logic components
- Timing constraints



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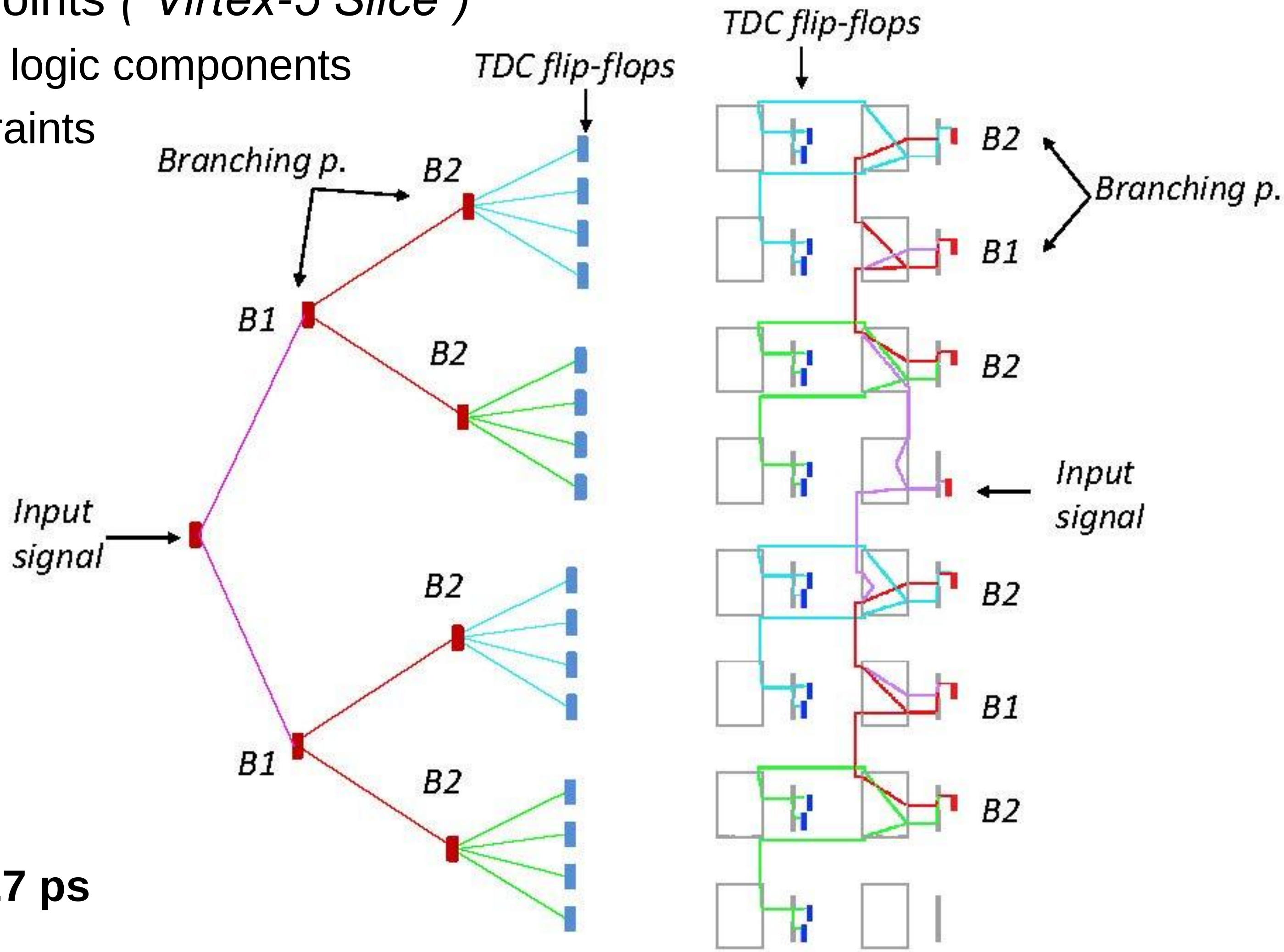
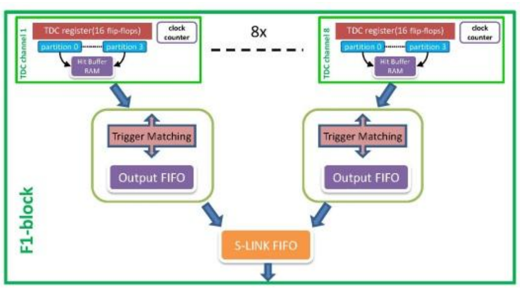


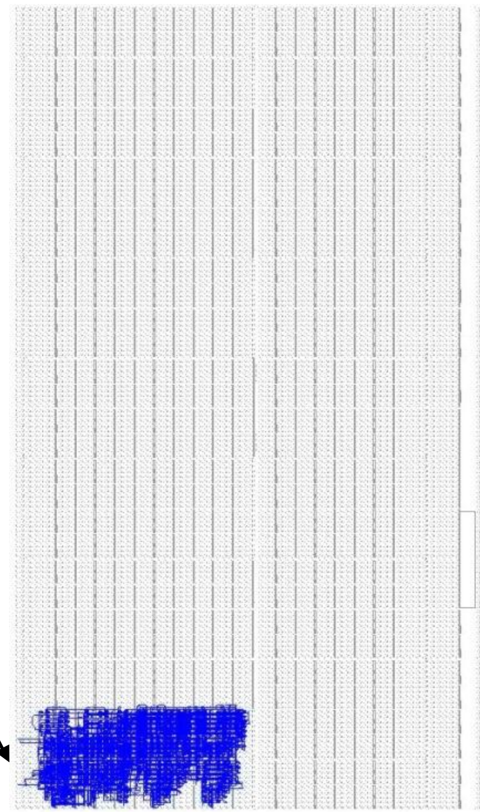
→ **Max. skew < 27 ps**

FPGA implementation

Incremental Design Reuse:

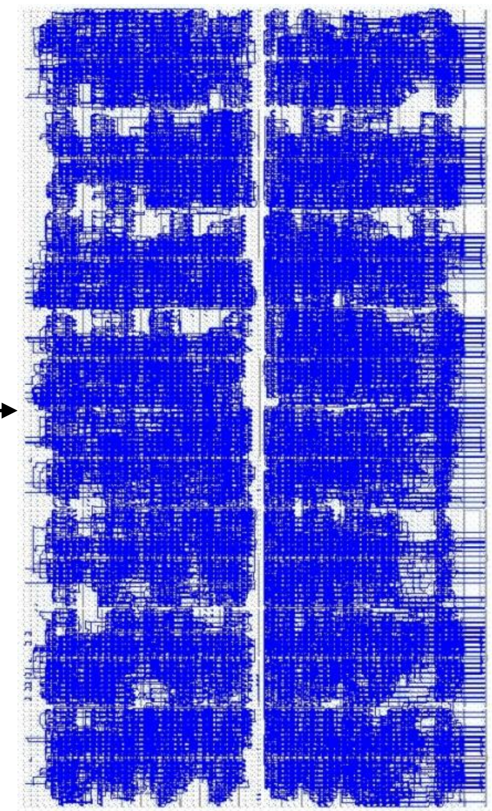
F1-block





Virtex-5 FPGA

$16\times$



Virtex-5 FPGA

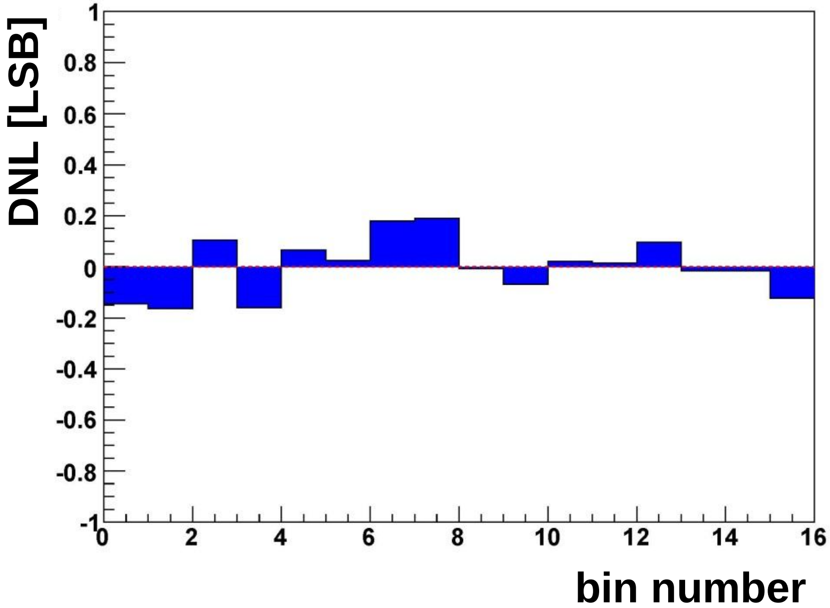
Measurement results

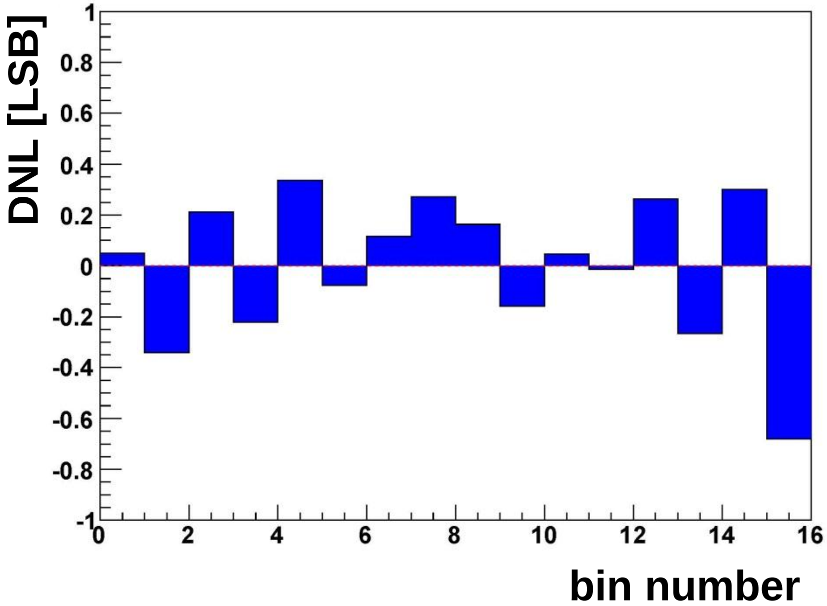
Differential Nonlinearity (DNL)

→ Statistical code-density test:

- N random hits
- Number of hits n_i in each TDC bin
- $DNL_i = \frac{n_i}{N/_{16}} - 1$

$1\text{LSB} = 160\text{ps}$





- *Minimum DNL:* $0.19 \times LSB$
- *Maximum DNL:* $0.68 \times LSB$

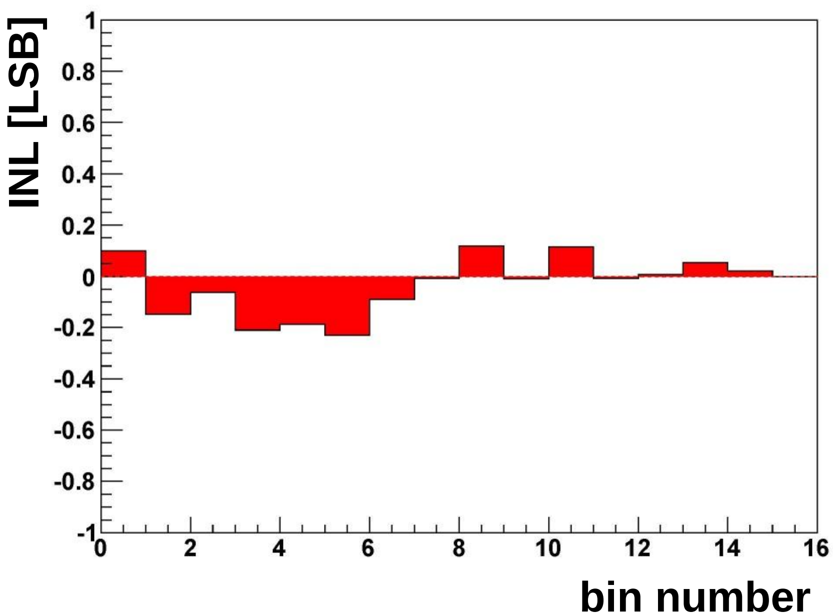
Measurement results

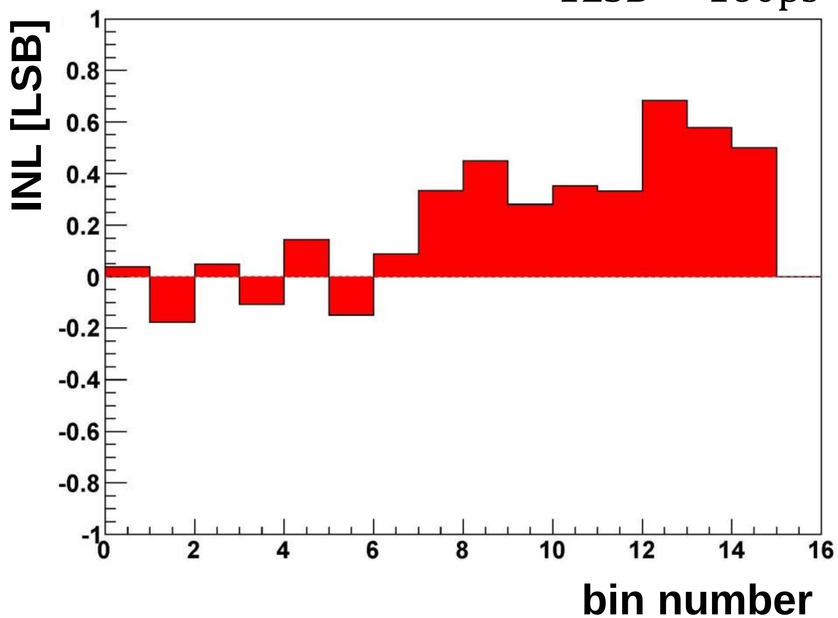
Integral Nonlinearity (INL)

→ $INL_i = \sum_{j=0}^{i} DNL_j, \quad i = 0,1,\dots,15$

- Deviation from ideal TDC transfer function
- Time resolution limited by INL

$1\mathrm{LSB} = 160\mathrm{ps}$

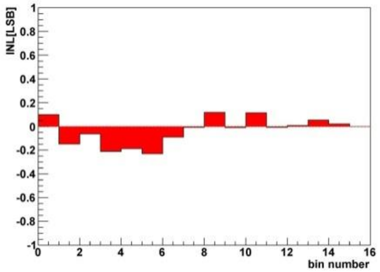




- *Minimum INL:* $0.23 \times LSB$
- *Maximum INL:* $0.68 \times LSB$

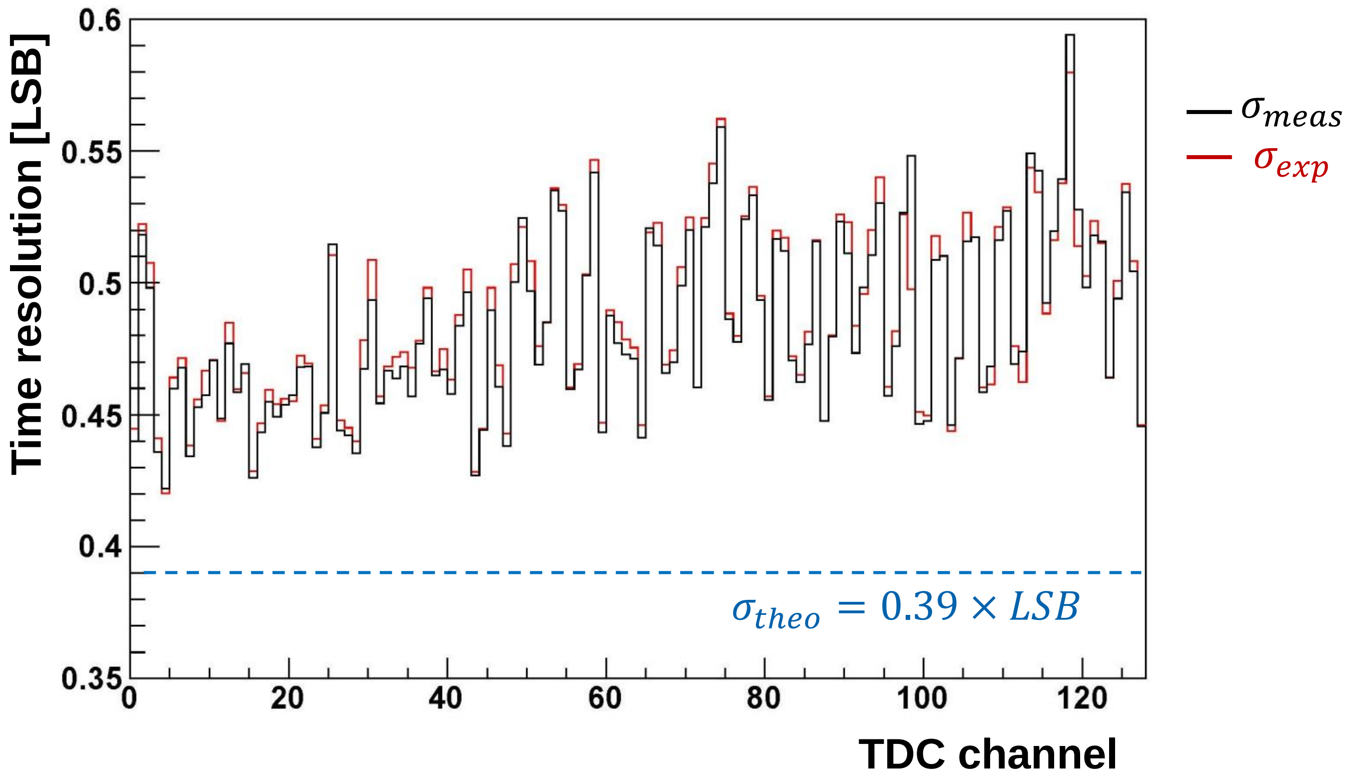
Measurement results

Time resolution



- Expected: $\sigma_{exp} = \sqrt{\sigma_{theo}^2 + 2 \times \sigma_{INL}^2}$,

$\sigma_{INL} = std.dev.(INL)$



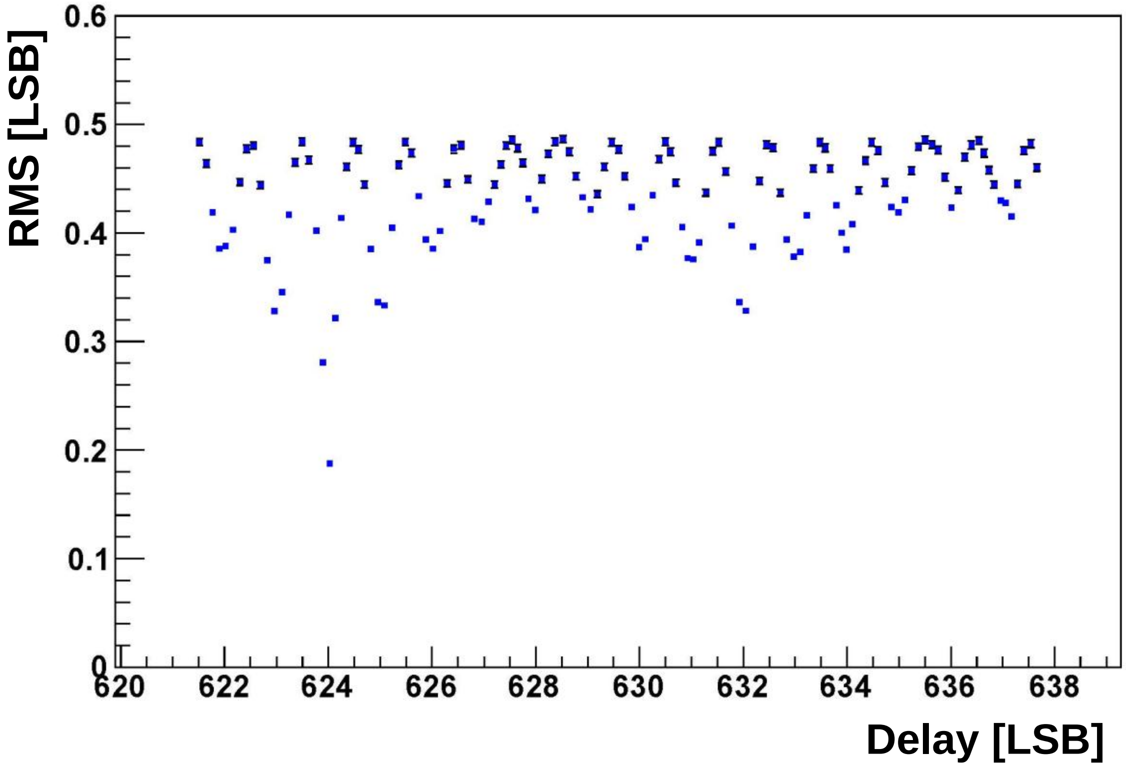
- *Minimum:* $0.42 \times LSB$ *Maximum:* $0.58 \times LSB$

Conclusion and Outlook

- Design objectives achieved:
  - ✓128 TDC channels implemented in single Xilinx Virtex-5 FPGA
  - ✓TDC bin size: $160\ ps$
  - ✓Time resolution $< 93\ ps$
  - ✓Virtex-5 SX95T device usage:
    - 43% *Flip-flops*
    - 27% *LUT*
    - 73% *Block RAM*
    - 22% *DSP Slice*

- In progress:
  - ✓Integrate 128 scaler channels into same design
  - ✓Migrate TDC design in low-cost FPGA as FE

Backup



RMS [LSB]
0.6
0.5
0.4
0.3
0.2
0.1
0
620
622
624
626
628
630
632
634
636
638
Delay [LSB]