GANDALF - Design of a Modular High Resolution Transient Recorder for High Energy Physics

S. Bartknecht, H. Fischer, F. Herrmann, K. Königsmann, L. Lauser, C. Schill, S. Schopferer, H. Wollny

***Abstract*–With present-day detectors in high energy physics one often faces short analog pulses with a typical length of a few nanoseconds length which may cover large dynamic ranges in amplitude. In many experiments both amplitude and timing information have to be measured with high accuracy. Additionally the data rate per readout channel can reach several MHz, which places strong demands on the separation of pile-up pulses.**

For such applications we have built the GANDALF transient recorder with a resolution of 12bit at a sampling rate of 1GS/s and an analog bandwidth of 500 MHz. Signals are digitized and processed by fast algorithms to extract pulse arrival times and amplitudes in real-time and to generate experiment trigger signals. With up to 16 analog channels, deep memories and a high data rate interface, this 6U-VME64x/VXS module is not only a dead time free readout system but also has huge numerical capabilities. These are provided by the implementation of a Virtex5-SXT FPGA, which is used to disentangle possible pile-up pulses and determine timing information with a time resolution in the picosecond range.

Recently the application spectrum has been extended by implementing a 128-channel time-to-digital converter inside the FPGA in combination with an appropriate input mezzanine card..

I. Introduction

THE COmmon Muon and Proton Apparatus for Structure and Spectroscopy (COMPASS) at the CERN SPS [1] is a state-of-the-art two stage magnetic spectrometer [2] with a flexible setup to allow for a rich variety of physics programs to be performed with secondary muon or hadron beams. Common to all measurements is the requirement for highest beam intensity and interaction rates with the needs of a high readout speed. Recently interest has been expressed for pursuing a dedicated measurement of Generalized Parton Distributions (GPD) [3]. For these measurements the existing COMPASS spectrometer will be extended by a new 2.4 m long liquid hydrogen target, which will be surrounded by a new recoil detector based on scintillating counters. The background induced by the passage of the beam through the target will yield rates of the order of a few MHz in the recoil detector counters. This imposes great demands on the digitization units and on a hardware trigger based on the recoil particle. For this purpose we have developed within the GANDALF framework a modular high speed and high resolution transient recorder system.

II. The GANDALF Framework

GANDALF (Fig. 1) is a 6U-VME64x/VXS carrier board which can host two mezzanine cards. It has been designed to cope with a variety of readout tasks in high energy and nuclear physics experiments. Two exchangeable mezzanine cards allow an employment of the system in very different applications such as analog-to-digital or time-to-digital conversions, coincidence matrix formation, fast pattern recognition or fast trigger generation. A schematic overview of the carrier board as transient recorder is provided in Figure 2. The heart of the board is a VIRTEX5-SXT FPGA which is connected to the mezzanine cards by several single ended and more than 110 differential signal interconnections. The data processing FPGA can perform complex calculations on data which have been sampled by ADC chips on the mezzanine cards.

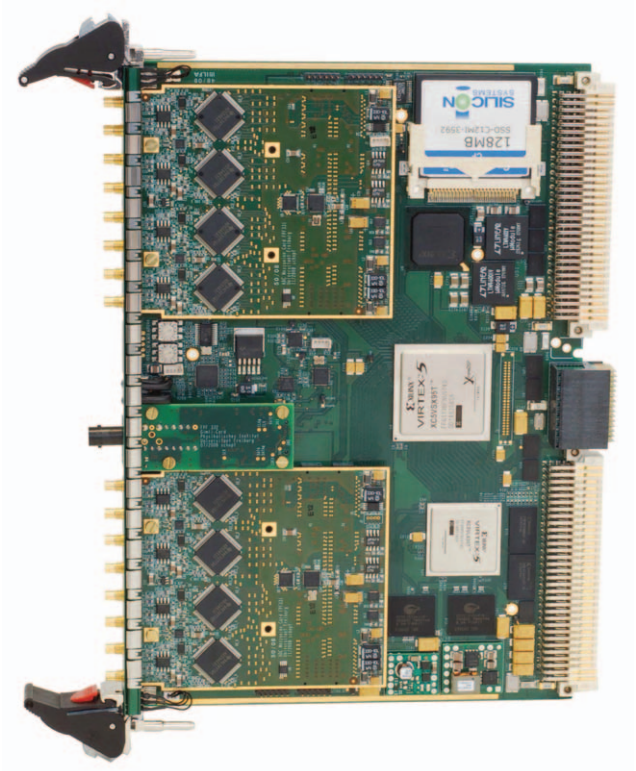

Figure 1: Picture of the GANDALF carrier board equipped with two ADC mezzanine cards. The center mezzanine card hosts an optical receiver for the COMPASS trigger and clock distribution system.

Fast and deep memory extensions of 144-Mbit QDRII+ and 4-Gbit DDR2 RAM are connected to a second Virtex5 FPGA. Both FPGAs are linked to each other by eight bidirectional high-speed Aurora lanes.

Connected to the VXS backplane GANDALF has 16 high-speed lanes for data transfer to a central VXS module, where the lanes of up to 18 GANDALF modules merge. This connection can be used for continuous transmission of the amplitudes and the time stamps from sampled signals to the VXS trigger processor, which then forms an input to the experiment-wide first-level trigger based on the energy loss and the time of flight in the recoil detector.

A dead-time free data output can either be realized by dedicated backplane link cards connected to each GANDALF P2-connector, i.e. following the 160 MByte/s SLink [4] or Ethernet protocol, or by the VME64x bus in block read mode [5] or by USB2.0 from the front panel.

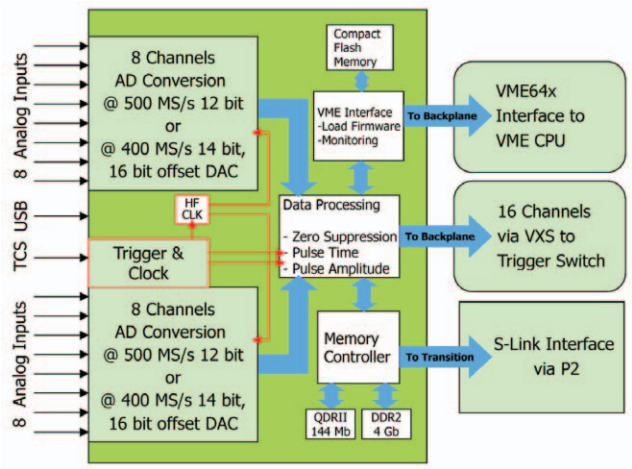

Figure 2: Block diagram of GANDALF as a transient recorder.

III. Analog-To-Digital Conversion

Two models of analog-to-digital converters (ADC) can be used with the GANDALF board, depending on the desired resolution. With the Texas Instruments models ADS5463 (12bit at 500MS/s) and ADS5474 (14bit at 400MS/s) we chose two of the fastest ADC chips that are currently available. Their low latency of only 3.5 clock cycles gives valuable time for the signal processing and the following trigger generation with its tight timing constraints defined by existent readout electronics.

The DC-coupled analog input circuit uses the differential amplifier LMH6552 from National Semiconductor and has a bandwidth of 500 MHz. It adapts the incoming single ended signal (e.g. from a PMT) to the dynamic range of the ADC while the baseline of each channel can be adjusted individually by 16-bit digital-to-analog converters (Fig. 3). Two adjacent channels can be interleaved to achieve an effective sampling rate of 1GS/s (800 MS/s with the ADS5474) at the cost of the number of channels per mezzanine card. In this time-interleaved mode the second ADC receives a sampling clock which is phase-shifted by 180 degree and the input signal is passively split to both channels. Thus the signal is sampled alternately by two ADCs.

On each ADC mezzanine card the high frequency sampling clock is generated by a digital clock synthesizer chip SI5326 from Silicon Labs, which comprises an integrated PLL consisting of an oscillator, a digital phase detector and a programmable loop filter. The experiment-wide 155.52-MHz clock, distributed by the COMPASS trigger and clock distribution system (TCS), is used as reference. Particular care has been paid to the design of the clock filter networks and the board layout to reach a time interval error smaller 730 fs [6], which is essential for high bandwidth sampling applications.

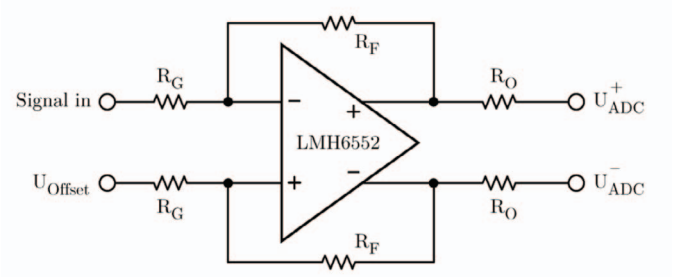

Figure 3: Schematic of the DC-coupled analog input circuit. For each channel U_{Offset} can be set by 16-bit DACs.

IV. Tests and Simulation

In experimental tests performed with a high precision function waveform generator (AFG-3252) and a selection of narrow band pass filters connected directly to the analog input we achieved an effective resolution on sample measurements of above 10.1 ENOB (ADS5463) and 10.6 ENOB (ADS5474) over an input frequency range up to 240 MHz. The result of these measurements is shown in Fig. 4 as a function of the frequency of the input analog signal and is expressed in dB as well as ENOB (effective number of bits).

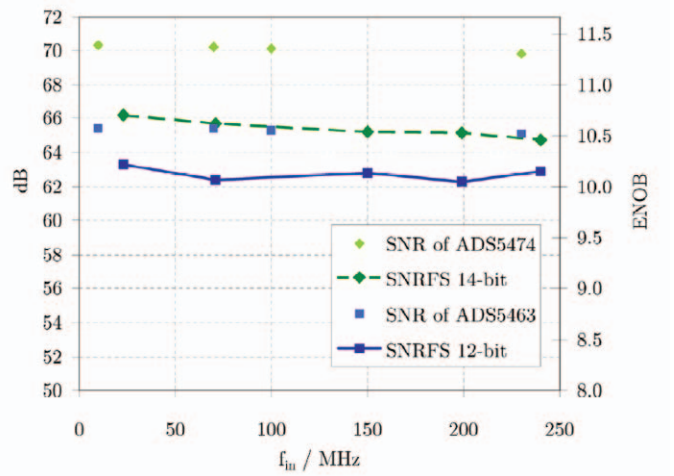

Figure 4: Signal-to-noise ratio (full-scale) and effective resolution of the 12-bit and 14-bit digitization units. Values from the ADC datasheets are given for comparison.

From a sampled pulse the FPGA can calculate the time of its occurrence using DSP-optimized numerical algorithms. With our knowledge of the sampling resolution extensive simulations aimed at the time resolution were performed.

Different algorithms were tested and optimized [7]. Our researches have shown that the digital constant fraction (dCFD) method is the best solution in timing calculation and numerical DSP efforts. Fig. 5 shows a simulated event and the principal of the dCFD. The signal shape of a by the GANDALF module recorded event is copied and inverted. After applying a fraction and delay value of the copied signal shape, the subtraction of both allows to receive a very precise timing information. By calculating the zero crossing we can reach a timing resolution below 50ps when choosing fraction factors of larger then 0.8 (Fig 6).

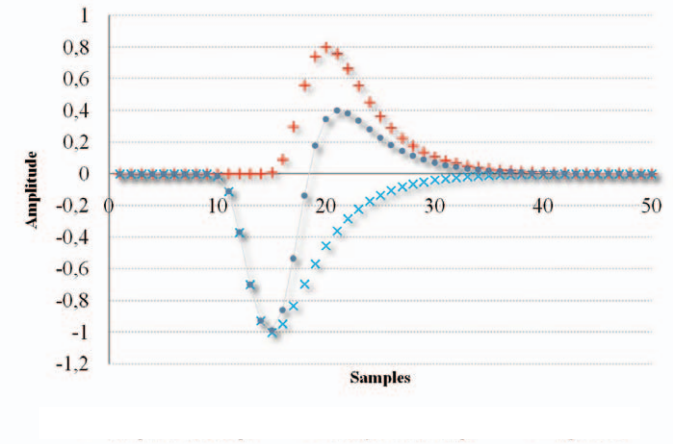

Figure 5: Example for signal processing with a digital Constant Fraction. The digitized pulse shape (blue crosses) is inverted, multiplied with a fraction factor and delayed by an integer value of samples (red crosses). The addition of both allow to determine timing information by calculating the zero fraction.

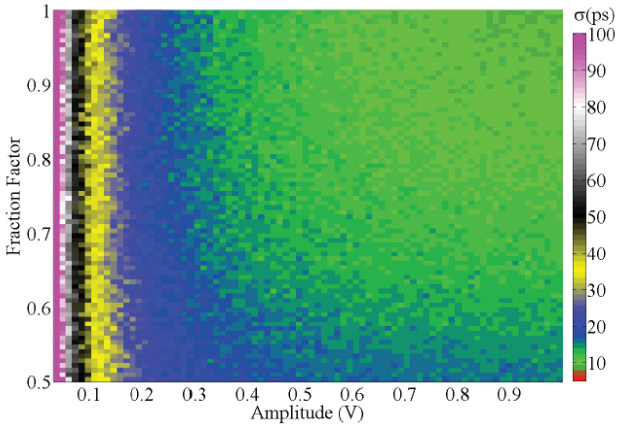

Figure 6: Timing resolution of the constant fraction algorithm in dependency of fraction factor and signal amplitude

The resolution on the time extracted from a pulse with different amplitudes and ~ 3 ns rise time, as expected from our detector, is shown in Figure 7.

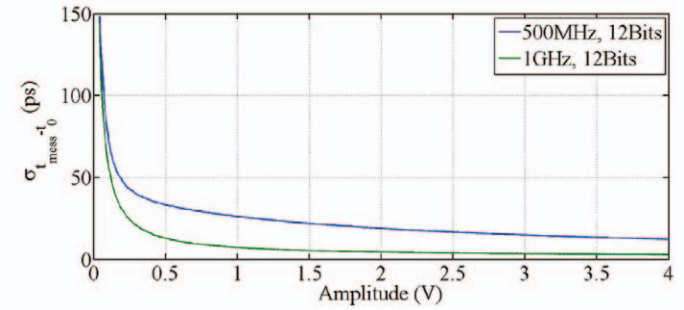

Figure 7: With our 12-bit, 1GS/s sampling ADC module a timing resolution of 17 ps can be achieved for pulses exceeding 10% of the dynamic range of the input signals.

V. Advanced Logic Functionalities

An additional digital mezzanine card (DMC) for logic signaling is has been designed as well. Each DMC allows an input data stream of 64 differential LVDS or LVPECL signals. As two mezzanine cards can be attached to one GANDALF module, combined logic functionalities on 128 channels can be performed. Every DMC also compromises two single ended NIM outputs and one NIM input for additional triggering or logic gates (Fig. 8).

We are researching different logic functionalities on these digital input channels, which are transferred from the DMCs input connectors to the central Virtex5 SXT FPGA via fast differential buffers with jitter values below 1ps. The high time resolution of the input transfer and the fast switching frequency of the processing FPGA allows us to implement time to digital conversion (TDC) functionalities inside the FPGA over these 128 channels.

The design of the modules also allows us to design a variety of digital measurement and trigger decision methods which are important in high energy physics. Design variations in the FPGA allow the implementation of scaler, mean timer and trigger matrices and combinations of them.

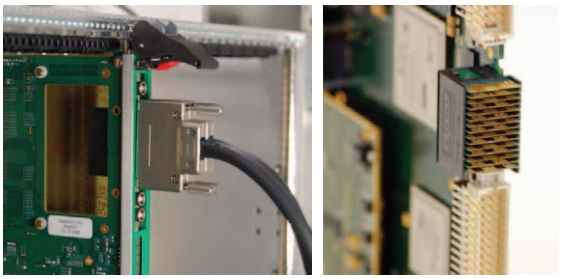

Figure 8: Left: A picture of the mounted DMC card and the mounted high density connector. Right: A picture of the high speed data transfer for VITA41.0 backplanes

The DMC cards are also designed to invert the direction of the differential input bus by a minimal change in the boards assembly. In this modus they can be used as logic output cards to produce signal pattern, which can be easily programmed inside the FPGA.

VI. Fast Trigger Generation

As shown in Fig. 2 the GANDALF module complies to the VITA 41.0 VXS specification. This standard is a powerful extension of the VME64x standard. It defines a new high data transfer bus on the backplane where the payload modules are connected to. Every GANDALF module has an additional high speed transition bus connector which connects the board with a central, so called trigger generator, module (Fig. 8). Therefore each GANDALF module can transfer its physical values, which are extracted from signal shape information, to a central trigger generator module. With the collected information from up to 18 GANDALF modules attached to one VXS crate the trigger generator is able to produce trigger information from up to 288 analog channels.

VII. Conclusion and Outlook

A low cost VME64x system aimed at digitizing and processing detector signals has been designed and implemented to our full satisfaction. The design is modular, consisting of a carrier board on which two mezzanine boards with either analog or digital inputs can be plugged. The ADC mezzanine cards have been characterized and show excellent performance over a wide input frequency range. Recently an additional type of mezzanine card with 64 digital inputs has been designed, which accepts LVDS and LVPECL signals over a VHDCI connector. An optional high-speed serial VXS backplane offers inter-module communication for sophisticated trigger processing possibly using a large number of detector channels.

The GANDALF transient recorder has been installed at the COMPASS experiment during a two-week DVCS pilot run in September 2009. Extensive data have been recorded in order to verify the performance of the hardware and the signal processing algorithms. In a forthcoming paper we will describe in detail the realization of GANDALF as a 128-channel time-to-digital converter module with 100 ps digitization units, comparable to the F1-TDC chip [8]. The TDC design is implemented inside the main FPGA which can host 128 channels of 500-MHz scalers at the same time.

VIII. References

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